

**512Mb DDR SDRAM**  
**HY5DU12422C(L)FP**  
**HY5DU12822C(L)FP**  
**HY5DU121622C(L)FP**

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## Revision History

Revision No.	History	Draft Date	Remark
1.0	First Version Release	Mar. 2005	
1.1	IDD specification revised	July 2005	
1.2	IDD6 specification revised	Feb. 2006	
1.3	State Diagram modified	Apr. 2006	

## DESCRIPTION

The HY5DU12422C(L)FP, HY5DU12822C(L)FP and HY5DU121622C(L)FP are a 536,870,912-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

This Hynix 512Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL\_2.

## FEATURES

- VDD, VDDQ = 2.5V ± 0.2V for DDR200, 266, 333  
VDD, VDDQ = 2.6V ± 0.1V for DDR400
- All inputs and outputs are compatible with SSTL\_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has two byte-wide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ)  
Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 2/2.5 (DDR200, 266, 333) and 3 (DDR400) supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh supported
- tRAS lock out function supported
- 8192 refresh cycles / 64ms
- 60 Ball FBGA Package Type
- Full and Half strength driver option controlled by EMRS
- Lead free (ROHS\* Compliant)

## ORDERING INFORMATION

Part No.	Configuration	Package
HY5DU12422C(L)FP-X*	128M x 4	60ball FBGA (Lead free)
HY5DU12822C(L)FP-X*	64M x 8	
HY5DU121622C(L)FP-X*	32M x 16	

\*X means speed grade

\*ROHS (Restriction Of Hazardous Substance)

## OPERATING FREQUENCY

Grade	Clock Rate		Remark (CL-tRCD-tRP)
-D43	200MHz@CL3		DDR400B (3-3-3)
- J	133MHz@CL2	166MHz@CL2.5	DDR333 (2.5-3-3)
- K	133MHz@CL2	133MHz@CL2.5	DDR266A (2-3-3)
- H	100MHz@CL2	133MHz@CL2.5	DDR266B (2.5-3-3)
- L	100MHz@CL2		DDR200 (2-2-2)























































