

# 128M(8Mx16) gDDR SDRAM

## HY5DU281622ETP

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## Revision History

Revision No.	History	Draft Date	Remark
0.1	Defined target spec.	July 2003	
0.2	Supports Lead free parts for each speed grade	Oct. 2003	
0.3	166Mhz speed bin delete, AC parameter change (trc_APCG at 200Mhz)	Jan. 2005	
1.0	Added Sentence to relate Power Up Sequence	Oct. 2005	

## DESCRIPTION

The Hynix HY5DU281622ETP is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the point-to-point applications which require high densities and high bandwidth.

The Hynix 8Mx16 DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL\_2.

## FEATURES

- 2.8V +/- 0.1V VDD and VDDQ power supply supports 400/375/350/333/300MHz
- 2.5V +/- 5% VDD and VDDQ power supply supports 275/250/200/166MHz
- All inputs and outputs are compatible with SSTL\_2 interface
- JEDEC Standard 400 mil x 875 mil 66 Pin TSOP II, with 0.65mm pin pitch
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (UDQS,LDQS)
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Data(DQ) and Write masks(DM) latched on the both rising and falling edges of the data strobe
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Write mask byte controls by DM (UDM,LDM)
- Programmable /CAS Latency 5, 4 and 3 are supported
- Programmable Burst Length 2, 4 and 8 with both sequential and interleave mode
- Internal 4 bank operation with single pulsed /RAS
- tRAS Lock-Out function are supported
- Auto refresh and self refresh are supported
- 4096 refresh cycles / 32ms
- Full strength, Half strength and Weak Impedance driver options controlled by EMRS

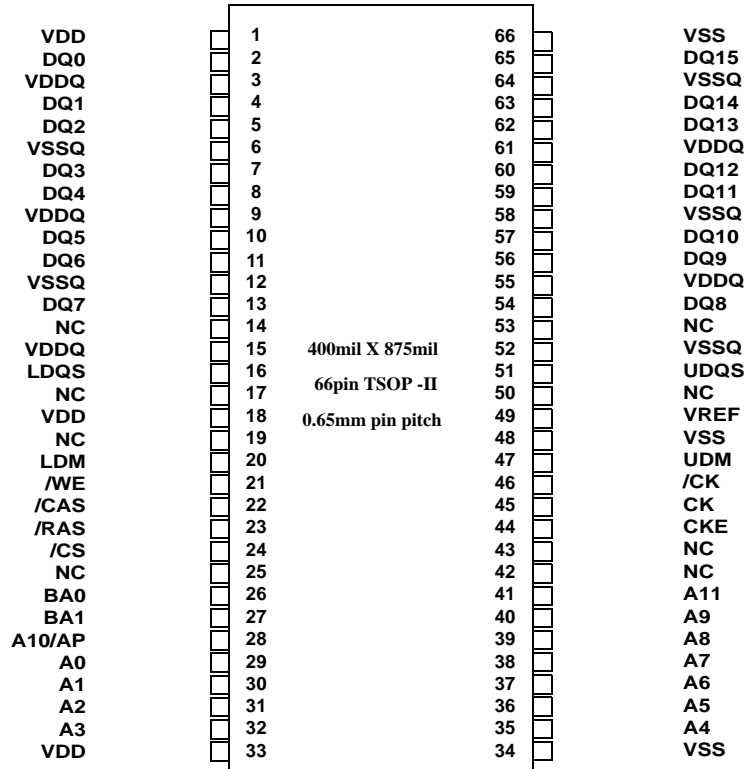
## ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Max Data Rate	interface	Package
HY5DU281622ETP-25	VDD/VDDQ=2.8V	400MHz	800Mbps/pin	SSTL_2	400 x 875mil <sup>2</sup> 66 Pin TSOP II
HY5DU281622ETP-26		375MHz	750Mbps/pin		
HY5DU281622ETP-28		350MHz	700Mbps/pin		
HY5DU281622ETP-30		333MHz	666Mbps/pin		
HY5DU281622ETP-33		300MHz	600Mbps/pin		
HY5DU281622ETP-36	VDD/VDDQ=2.5V	275MHz	550Mbps/pin		
HY5DU281622ETP-4		250MHz	500Mbps/pin		
HY5DU281622ETP-5		200MHz	400Mbps/pin		

Note) Hynix supports Lead free parts for each speed grade with same specification, except Lead free material.

We'll add "P" character after "T" for Pb free product. For example, the part number of 300MHz Lead free Product is HY5DU281622ETP-33.

**PIN CONFIGURATION (Top View)**



**ROW AND COLUMN ADDRESS TABLE**

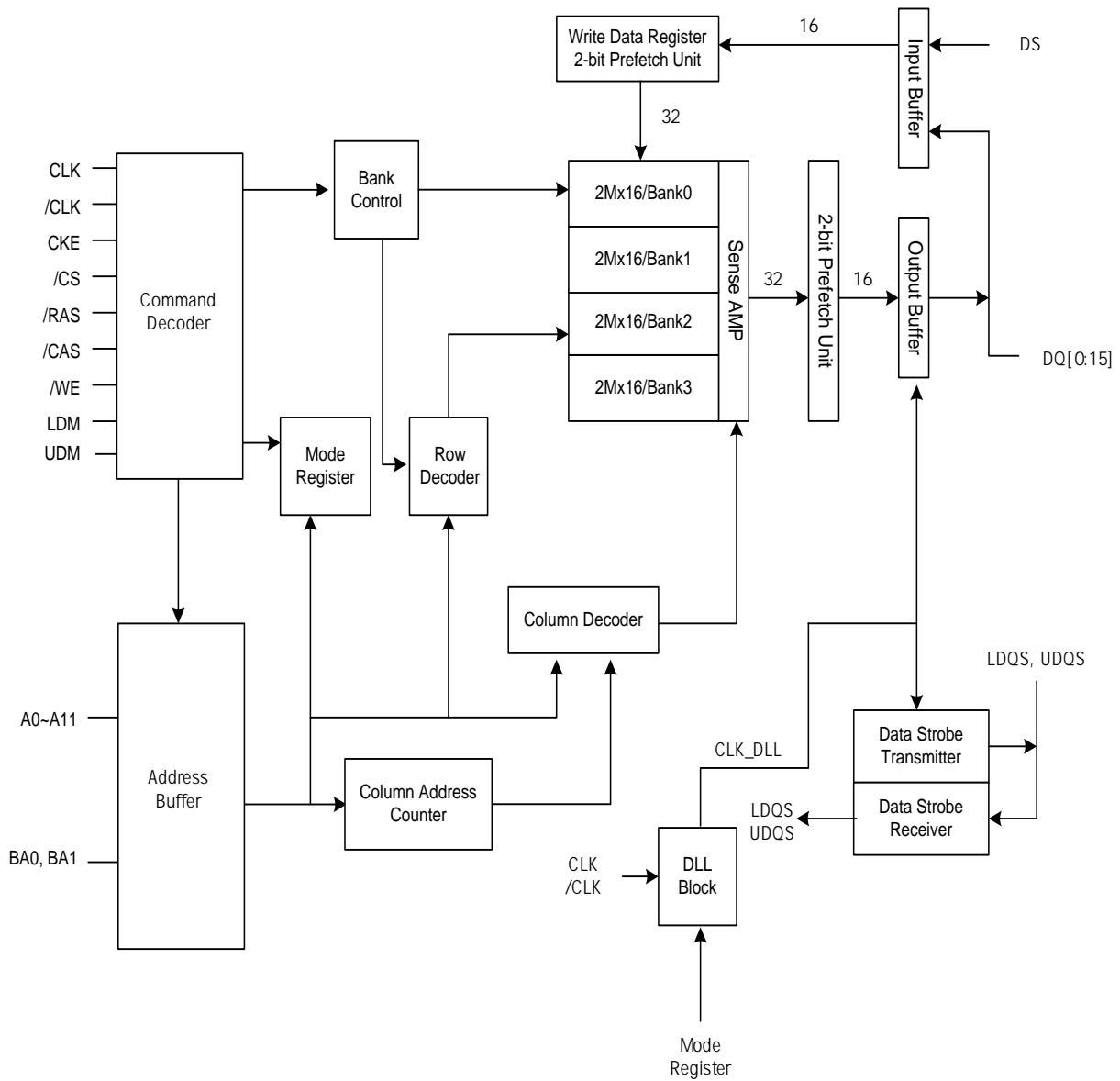
ITEMS	8Mx16
Organization	2M x 16 x 4banks
Row Address	A0 - A11
Column Address	A0-A8
Bank Address	BA0, BA1
Auto Precharge Flag	A10
Refresh	4K

**PIN DESCRIPTION**

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry and exit. CKE is asynchronous for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
UDM, LDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15
UDQS, LDQS	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15
DQ0 ~ DQ15	I/O	Data input / output pin : Data Bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

**FUNCTIONAL BLOCK DIAGRAM**

4Banks x 2Mbit x 16 I/O Double Data Rate Synchronous DRAM



**SIMPLIFIED COMMAND TRUTH TABLE**

Command	CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA	Note
Extended Mode Register Set	H	X	L	L	L	L	OP code			1,2
Mode Register Set	H	X	L	L	L	L	OP code			1,2
Device Deselect	H	X	H	X	X	X	X			1
No Operation			L	H	H	H				
Bank Active	H	X	L	L	H	H	RA		V	1
Read	H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge								H		1,3
Write	H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge								H		1,4
Precharge All Banks	H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank								L	V	1
Read Burst Stop	H	X	L	H	H	L	X			1
Auto Refresh	H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X		1
	Exit	L	H	H	X	X	X			1
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	H	H	H			1
	Exit	L	H	H	X	X	X			1
				L	H	H	H			1
Active Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	V	V	V			1
	Exit	L	H	X			1			

( H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation )

**Note :**

- UDM, LDM states are Don't Care. Refer to below Write Mask Truth Table.(note 6)
- OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
- If a Read with Auto-precharge command is detected by memory component in CK(n), then there will be no command presented to activate bank until CK(n+BL/2+tRP).
- If a Write with Auto-precharge command is detected by memory component in CK(n), then there will be no command presented to activate bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechagre delay(tDPL) which is also called Write Recovery Time(tWR) is needed to guarantee that the last data have been completely written.
- If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.
- In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of  $V_{IHmin} \sim V_{ILmax}$

**WRITE MASK TRUTH TABLE**

Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADDR	A8/ AP	BA	Note
Data Write	H	X	X	L		X		1,2,3
Data-In Mask	H	X	X	H		X		1,2,3

**Note :**

1. Write Mask command masks burst write data with reference to UDQS/LDQS and it is not related with read data.
2. LDM corresponds to the data on DQ0-Q7 and UDM corresponds to the data on DQ8-Q15
3. In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of  $V_{IHmin} \sim V_{ILmax}$

**OPERATION COMMAND TRUTH TABLE - I**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DSEL	NOP or power down <sup>3</sup>
	L	H	H	H	X	NOP	NOP or power down <sup>3</sup>
	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>4</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>4</sup>
	L	L	H	H	BA, RA	ACT	Row Activation
	L	L	H	L	BA, AP	PRE/PALL	NOP
	L	L	L	H	X	AREF/SREF	Auto Refresh or Self Refresh <sup>5</sup>
ROW ACTIVE	L	L	L	L	OPCODE	MRS	Mode Register Set
	H	X	X	X	X	DSEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	Begin read : optional AP <sup>6</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	Begin write : optional AP <sup>6</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4</sup>
	L	L	H	L	BA, AP	PRE/PALL	Precharge <sup>7</sup>
READ	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Terminate burst
	L	H	L	H	BA, CA, AP	READ/READAP	Term burst, new read:optional AP <sup>8</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4</sup>
WRITE	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
WRITE	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	Term burst, new read:optional AP <sup>8</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	Term burst, new write:optional AP

**OPERATION COMMAND TRUTH TABLE - II**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4</sup>
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
READ WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>10</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>10</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4,10</sup>
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>4,10</sup>
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
WRITE AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>10</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>10</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4,10</sup>
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>4,10</sup>
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
PRE-CHARGE	H	X	X	X	X	DSEL	NOP-Enter IDLE after tRP
	L	H	H	H	X	NOP	NOP-Enter IDLE after tRP
	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>4,10</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>4,10</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4,10</sup>
	L	L	H	L	BA, AP	PRE/PALL	NOP-Enter IDLE after tRP
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>

**OPERATION COMMAND TRUTH TABLE - III**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
ROW ACTIVATING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tRCD
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tRCD
	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>4,10</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>4,10</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4,9,10</sup>
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>4,10</sup>
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
WRITE RECOVERING	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tWR
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tWR
	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4,10</sup>
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>4,11</sup>
WRITE RECOVERING WITH AUTOPRE-CHARGE	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
	H	X	X	X	X	DSEL	NOP - Enter precharge after tDPL
	L	H	H	H	X	NOP	NOP - Enter precharge after tDPL
	L	H	H	L	X	BST	ILLEGAL <sup>4</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>4,8,10</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>4,10</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>4,10</sup>
REFRESHING	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>4,11</sup>
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
	H	X	X	X	X	DSEL	NOP - Enter IDLE after tRC
REFRESHING	L	H	H	H	X	NOP	NOP - Enter IDLE after tRC
	L	H	H	L	X	BST	ILLEGAL <sup>11</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>11</sup>

**OPERATION COMMAND TRUTH TABLE - IV**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>11</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>11</sup>
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>11</sup>
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
	L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>
MODE REGISTER ACCESSING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tMRD
	L	H	H	H	X	NOP	NOP - Enter IDLE after tMRD
	L	H	H	L	X	BST	ILLEGAL <sup>11</sup>
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL <sup>11</sup>
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL <sup>11</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>11</sup>
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL <sup>11</sup>
	L	L	L	H	X	AREF/SREF	ILLEGAL <sup>11</sup>
L	L	L	L	OPCODE	MRS	ILLEGAL <sup>11</sup>	

**Note :**

- H - Logic High Level, L - Logic Low Level, X - Don't Care, V - Valid Data Input, BA - Bank Address, AP - AutoPrecharge Address, CA - Column Address, RA - Row Address, NOP - NO Operation.(see note 12)
- All entries assume that CKE was active(high level) during the preceding clock cycle.
- If both banks are idle and CKE is inactive(low level), then in power down mode.
- Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA) depending on the state of that bank.
- If both banks are idle and CKE is inactive(low level), then self refresh mode.
- Illegal if tRCD is not met.
- Illegal if tRAS is not met.
- Must satisfy bus contention, bus turn around, and/or write recovery requirements.
- Illegal if tRRD is not met.
- Illegal for single bank, but legal for other banks in multi-bank devices.
- Illegal for all banks.
- In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of  $V_{IHmin} \sim V_{ILmax}$

**CKE FUNCTION TRUTH TABLE**

Current State	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	/ADD	Action
SELF REFRESH <sup>1</sup>	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	H	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue self refresh
POWER DOWN <sup>2</sup>	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit power down, enter idle
	L	H	L	H	H	H	X	Exit power down, enter idle
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue power down mode
ALL BANKS IDLE <sup>4</sup>	H	H	X	X	X	X	X	See operation command truth table
	H	L	L	L	L	H	X	Enter self refresh
	H	L	H	X	X	X	X	Exit power down
	H	L	L	H	H	H	X	Exit power down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
ANY STATE OTHER THAN ABOVE	H	H	X	X	X	X	X	See operation command truth table
	H	L	X	X	X	X	X	ILLEGAL <sup>5</sup>
	L	H	X	X	X	X	X	INVALID
	L	L	X	X	X	X	X	INVALID

**Note :**

When CKE=L, all DQ and UDQS/LDQS should be in Hi-Z state.

1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing any command.
2. All commands can be stored after 2 clocks from low to high transition of CKE.
3. Illegal, if CK is suspended or stopped during the power down mode.
4. Self refresh can be asserted only from the all banks idle state.
5. Disabling CK may cause malfunction of any banks which are in active state.



## POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD and VDDQ simultaneously, and then to VREF (and to the system VTT).

VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device.

VREF can be applied any time after VDDQ but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL\_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. After the DLL reset, tXSRD(DLL locking time) should be satisfied for read command. After the Mode Register set command, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated low (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.)

No power sequencing is specified during power up or power down given the following criteria :

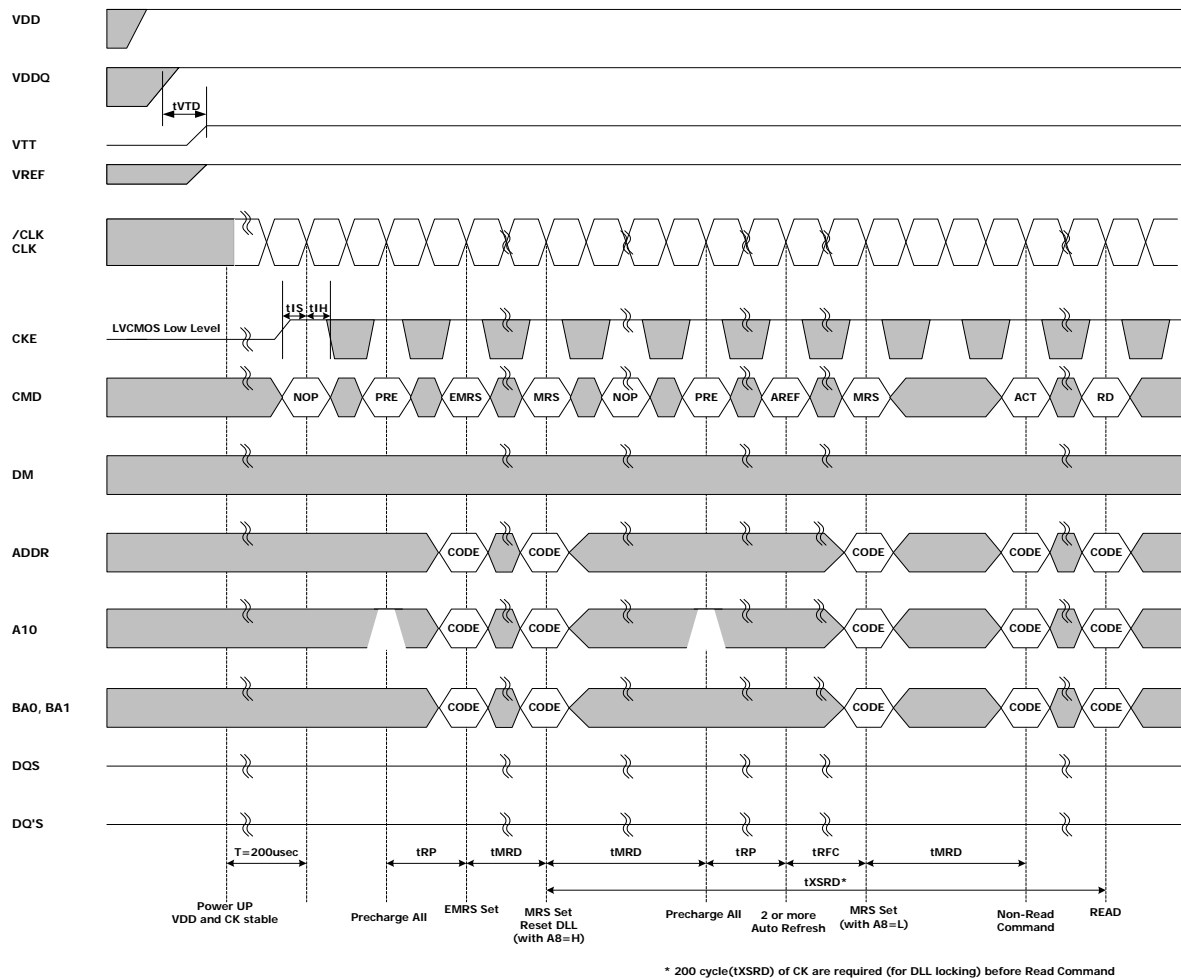
- VDD and VDDQ are driven from a single power converter output.
- VTT is limited to 1.35V.
- VREF tracks VDDQ/2.
- If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up :

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

2. Start clock and maintain stable clock for a minimum of 200µsec.
3. After stable power and clock, apply NOP or DESELECT conditionS and take CKE high.
4. Following the NOP command, a PRECHARGE ALL command should be applied
5. Issue Extended Mode Register Set (EMRS) to enable DLL.
6. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=high. (An additional 200 cycles(tXSRD) of clock are required for locking DLL)

7. Issue Precharge commands for all banks of the device.
8. Issue 2 or more Auto Refresh commands.
9. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low.

**Power-Up Sequence**



**Note)**

1. VTT is not applied directly to the device; however,  $t_{VTD}$  should be greater than or equal to zero to avoid device latch-up. VDDQ, VTT and VREF must be equal to or less than  $VDD + 0.3V$ . Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0V. Once initialized, including self refresh mode, VREF must always be powered within specified range.
2. The Power Voltage ramp time between initial VDD and VDDmin must be no less than 3ms.
3. The Initial VDD must be maintained under 100mV.



































