

# 128Mb DDR SDRAM

## HY5DU281622ET-D43/D4

## Revision History

Revision No.	History	Draft Date	Remark
0.1	Datasheet Release in Preliminary version	Aug. 2003	
0.2	1) Separate x16 component only 2) Updated IDD values	Jun. 2004	
0.3	Editorial Change	Jul. 2004	
0.4	1) Updated High, Low Current Level of Output Driver Strength in DC OPERATING CONDITIONS 2) Corrected 6th note and Added 7th note in DC OPERATING CONDITIONS 3) Editorial Changes	Aug. 2004	
0.5	State Diagram modified	Apr. 2006	

## DESCRIPTION

The HY5DU281622ET-D43/D4 are a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

This Hynix 128Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL\_2.

## FEATURES

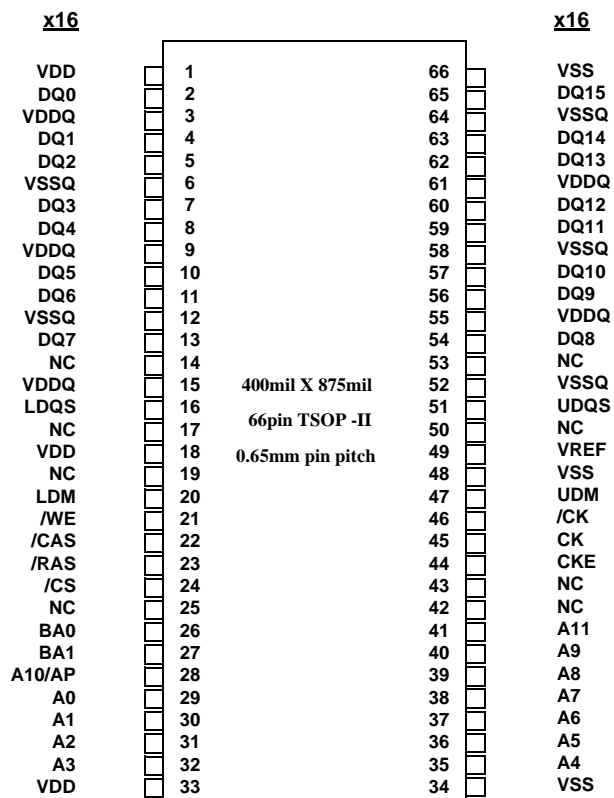
- VDD, VDDQ = 2.6V +/- 0.1V
- All inputs and outputs are compatible with SSTL\_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- Two byte-wide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- On chip DLL aligns DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable /CAS latency 2/ 2.5/ 3 supported
- Programmable burst length 2/ 4/ 8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh are supported
- tRAS lock out function is supported
- 4096 refresh cycles / 64ms
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Full and Half strength driver options are controlled by EMRS

## ORDERING INFORMATION

Part No.	Configuration	Package
HY5DU281622ET-D43	8Mx16	400mil 66 pin
HY5DU281622ET-D4		TSOP II

## OPERATING FREQUENCY

Grade	CL3	Remark (CL-tRCD-tRP)
- D43	200MHz	DDR400 (3-3-3)
- D4	200MHz	DDR400 (3-4-4)

**PIN CONFIGURATION**

**ROW AND COLUMN ADDRESS TABLE**

ITEMS	8Mx16
Organization	2M x 16 x 4banks
Row Address	A0 - A11
Column Address	A0-A8
Bank Address	BA0, BA1
Auto Precharge Flag	A10
Refresh	4K

**PIN DESCRIPTION**

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied.
/CS	Input	Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin: Data bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

















































