



128Mb DDR SDRAM

HY5DU281622FTP

Revision History

Revision No.	History	Draft Date	Remark
0.01	First version for internal review	Feb. 2006	
0.02	State Diagram modified	Apr. 2006	
0.03	Defined : IDD value	Apr. 2006	

DESCRIPTION

The HY5DU281622FT(P) is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

This Hynix 128Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

FEATURES

- $V_{DD}, V_{DDQ} = 2.3V \text{ min} \sim 2.7V \text{ max}$
(Typical 2.5V Operation +/- 0.2V for DDR266, 333)
- $V_{DD}, V_{DDQ} = 2.4V \text{ min} \sim 2.7V \text{ max}$
(Typical 2.6V Operation +0.1/- 0.2V for DDR400 and 400Mbps/pin product)
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has two byte-wide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ)
Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 2/2.5 (DDR266, 333) and 3 (DDR400 and 400Mbps/pin product) supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh supported
- tRAS lock out function supported
- 4096 refresh cycles/64ms
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Lead free (*ROHS Compliant)

ORDERING INFORMATION

Part No.	Configuration	Package
HY5DU281622F(L)TP-X*	8Mx16	400mil 66pin TSOP-II**

* X means speed grade

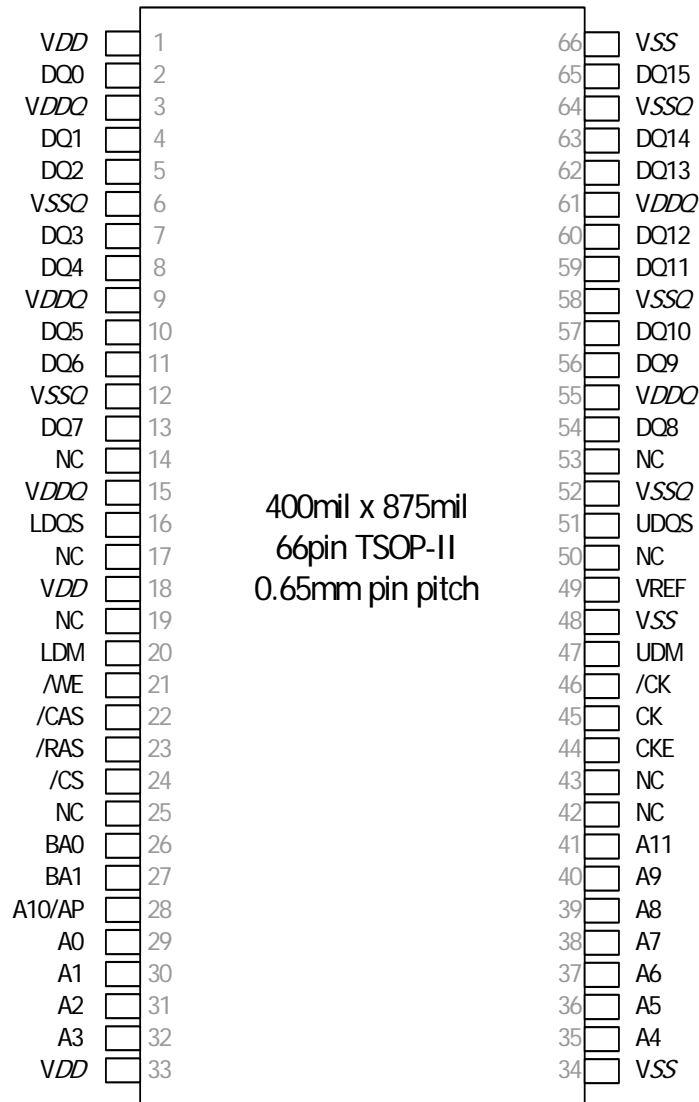
** Lead-free product

*ROHS (Restriction Of Hazardous Substances)

OPERATING FREQUENCY

Grade	Clock Rate		Remark
-5	200MHz@CL3		400Mbps/pin (maximum Date rate)
-D43	200MHz@CL3		DDR400B (3-3-3)
-D4	200MHz@CL3		DDR400 (3-4-4)
-J	133MHz@CL2	166MHz @CL2.5 & @CL3	DDR333 (2.5-3-3) DDR333 (3-3-3)
-K	133MHz@CL2	133MHz@CL2.5	DDR266A (2-3-3)
-H	100MHz@CL2	133MHz@CL2.5	DDR266B (2.5-3-3)

PIN CONFIGURATION



ROW AND COLUMN ADDRESS INFORMATION

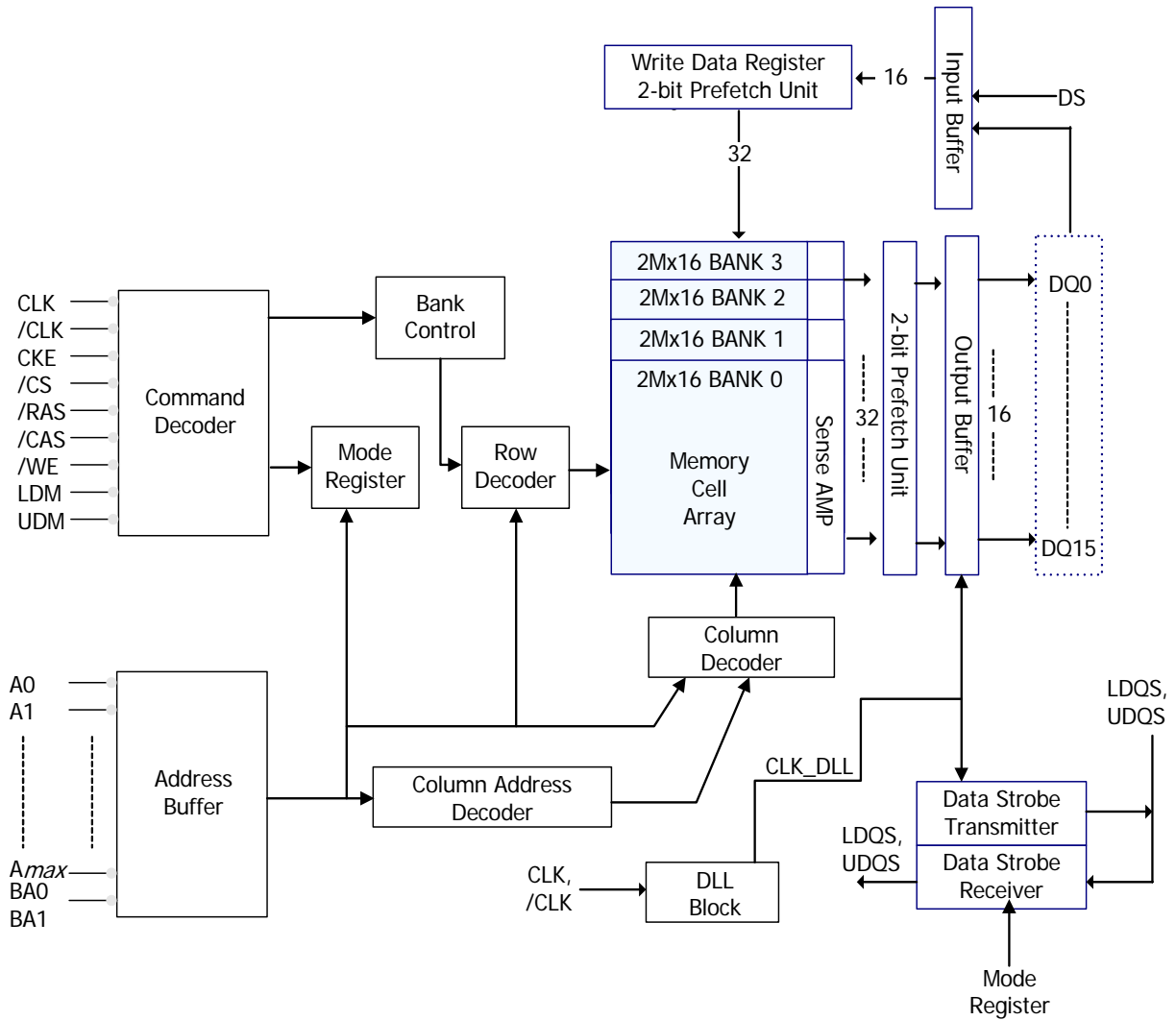
- Organization : 2M x 16 x 4banks
- Row Address : A0 - A11
- Column Address : A0 - A8
- Bank Address : BA0, BA1
- Auto Precharge Flag : A10
- Refresh : 4K

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied.
/CS	Input	Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when Chip Select is registered high. Chip Select provides for external bank selection on systems with multiple banks. Chip Select is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin: Data bus
VDD / VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ / VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

Functional Block Diagram (8M x16)

4Banks x 2Mbit x 16I/O Double Data Rate Synchronous DRAM



SIMPLIFIED COMMAND TRUTH TABLE

Command	CKEn-1	CKEn	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR	A10 /AP	BA	Note
Extended Mode Register Set	H	X	L	L	L	L	OP code		1,2	
Mode Register Set	H	X	L	L	L	L	OP code		1,2	
Device Deselect	H	X	H	X	X	X	X		1	
No Operation			L	H	H	H				
Bank Active	H	X	L	L	H	H	RA	V	1	
Read	H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge								H		1,3
Write	H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge								H		1,4
Precharge All Banks	H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank								L	V	1
Read Burst Stop	H	X	L	H	H	L	X		1	
Auto Refresh	H	H	L	L	L	H	X		1	
Self Refresh	Entry	H	L	L	L	L	H	X		1
	Exit	L	H	H	X	X	X			1
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	H	H	H			1
	Exit	L	H	H	X	X	X			1
				L	H	H	H			1
Active Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	V	V	V			1
	Exit	L	H	X						1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. UDM, LDM states are Don't Care. Refer to below Write Mask Truth Table.(note 6)
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Auto-precharge command is detected by memory component in CK(n), then there will be no command presented to activate bank until CK(n+BL/2+tRP).
4. If a Write with Auto-precharge command is detected by memory component in CK(n), then there will be no command presented to activate bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time(tWR) is needed to guarantee that the last data have been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.
6. In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of $V_{IHmin} \sim V_{ILmax}$

WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADD R	A10/ AP	BA	Note
Data Write	H	X	X	L		X		1,2
Data-In Mask	H	X	X	H		X		1,2

Note :

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strokes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.
2. In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of $V_{IHmin} \sim V_{ILmax}$

POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to *VDD*, then to *VDDQ*, and finally to *VREF* (and to the system *VTT*). *VTT* must be applied after *VDDQ* to avoid device latch-up, which may cause permanent damage to the device. *VREF* can be applied anytime after *VDDQ*, but is expected to be nominally coincident with *VTT*. Except for *CKE*, inputs are not recognized as valid until after *VREF* is applied. *CKE* is an *SSTL_2* input, but will detect an *LVC*MOS LOW level after *VDD* is applied. Maintaining an *LVC*MOS LOW level on *CKE* during power-up is required to guarantee that the *DQ* and *DQS* outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a *DESELECT* or *NOP* command should be applied, and *CKE* should be brought HIGH. Following the *NOP* command, a *PRECHARGE ALL* command should be applied. Next a *EXTENDED MODE REGISTER SET* command should be issued for the Extended Mode Register, to enable the *DLL*, then a *MODE REGISTER SET* command should be issued for the Mode Register, to reset the *DLL*, and to program the operating parameters. After the *DLL* reset, *txSRD*(*DLL* locking time) should be satisfied for read command. After the Mode Register set command, a *PRECHARGE ALL* command should be applied, placing the device in the all banks idle state.

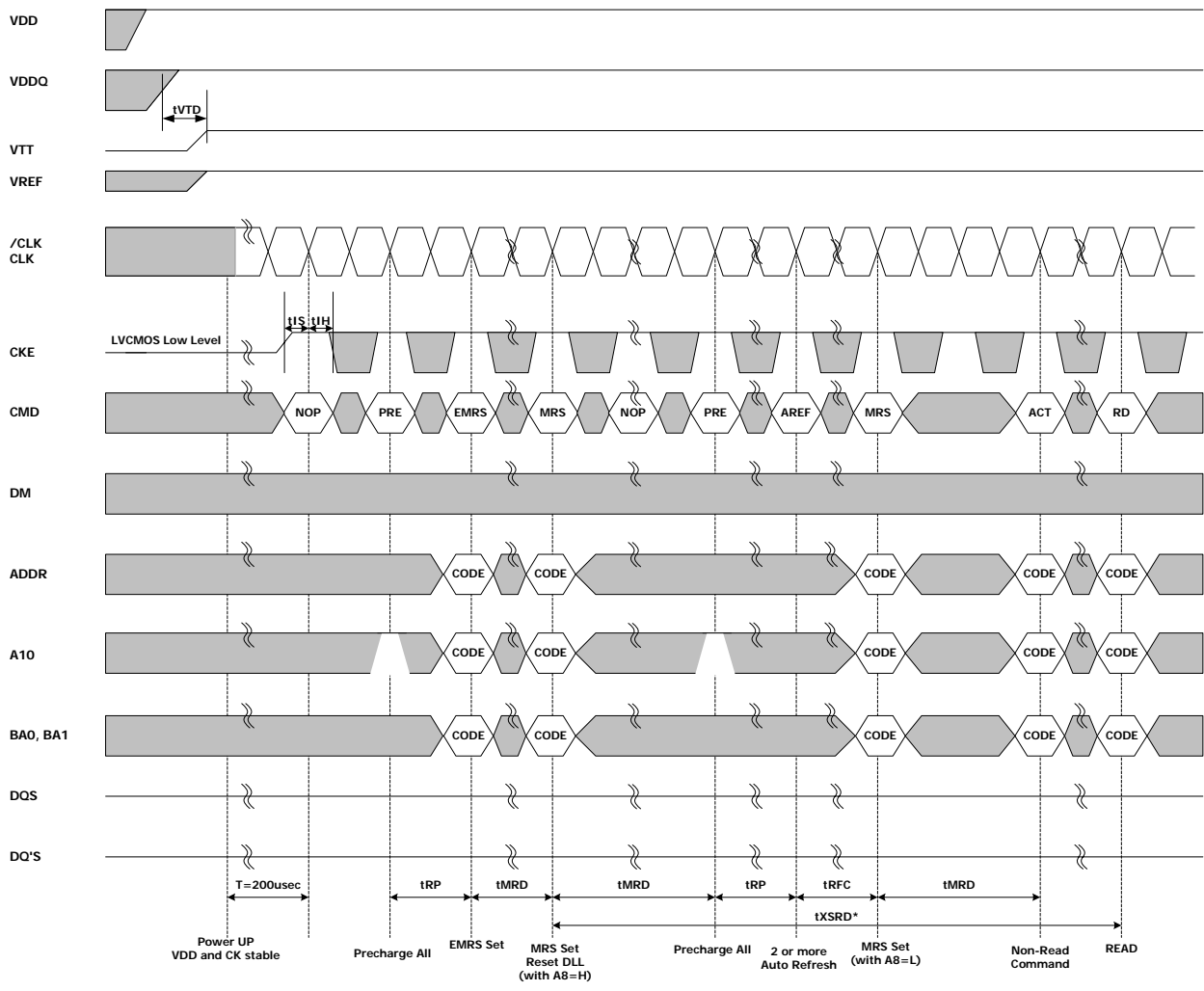
Once in the idle state, two *AUTO REFRESH* cycles must be performed. Additionally, a *MODE REGISTER SET* command for the Mode Register, with the reset *DLL* bit deactivated low (i.e. to program operating parameters without resetting the *DLL*) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - *VDD*, *VDDQ*, *VTT*, *VREF* in the following power up sequencing and attempt to maintain *CKE* at *LVC*MOS low state. (All the other input pins may be undefined.)
 - *VDD* and *VDDQ* are driven from a single power converter output.
 - *VTT* is limited to $1.44V$ (reflecting $VDDQ(max)/2 + 50mV$ *VREF* variation + $40mV$ *VTT* variation).
 - *VREF* tracks $VDDQ/2$.
 - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
<i>VDDQ</i>	After or with <i>VDD</i>	$< VDD + 0.3V$
<i>VTT</i>	After or with <i>VDDQ</i>	$< VDDQ + 0.3V$
<i>VREF</i>	After or with <i>VDDQ</i>	$< VDDQ + 0.3V$

2. Start clock and maintain stable clock for a minimum of 200usec.
3. After stable power and clock, apply *NOP* condition and take *CKE* high.
4. Issue Extended Mode Register Set (*EMRS*) to enable *DLL*.
5. Issue Mode Register Set (*MRS*) to reset *DLL* and set device to idle state with bit *A8*=high. (An additional 200 cycles(*txSRD*) of clock are required for locking *DLL*)
6. Issue Precharge commands for all banks of the device.
7. Issue 2 or more Auto Refresh commands.
8. Issue a Mode Register Set command to initialize the mode register with bit *A8* = Low

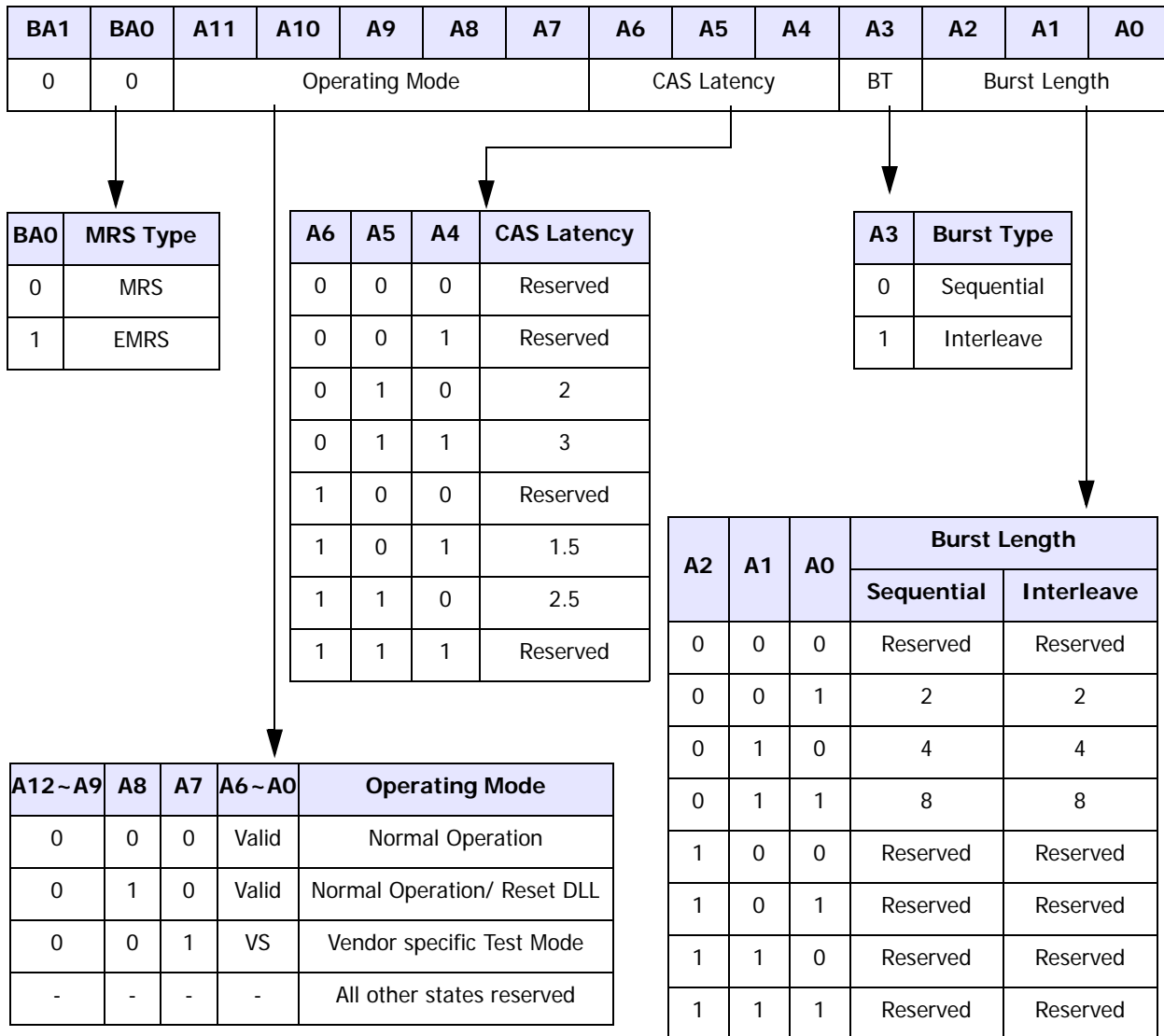
Power-Up Sequence



* 200 cycle(t_{XSRD}) of CK are required (for DLL locking) before Read Command

MODE REGISTER SET (MRS)

The mode register is used to store the various operating modes such as /CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is programmed via MRS command. This command is issued by the low signals of /RAS, /CAS, /CS, /WE and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Two cycles are required to write the data in mode register. During the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until reset by another MRS command.



BURST DEFINITION

Burst Length	Starting Address (A2,A1,A0)	Sequential	Interleave
2	XX0	0, 1	0, 1
	XX1	1, 0	1, 0
4	X00	0, 1, 2, 3	0, 1, 2, 3
	X01	1, 2, 3, 0	1, 0, 3, 2
	X10	2, 3, 0, 1	2, 3, 0, 1
	X11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BURST LENGTH & TYPE

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2 -Ai when the burst length is set to four and by A3 -Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table

CAS LATENCY

The Read latency or CAS latency is the delay in clock cycles between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks for DDR266/333 and 3 clocks for DDR400.

If a Read command is registered at clock edge n , and the latency is m clocks, the data is available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DLL RESET

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before an any command can be issued.

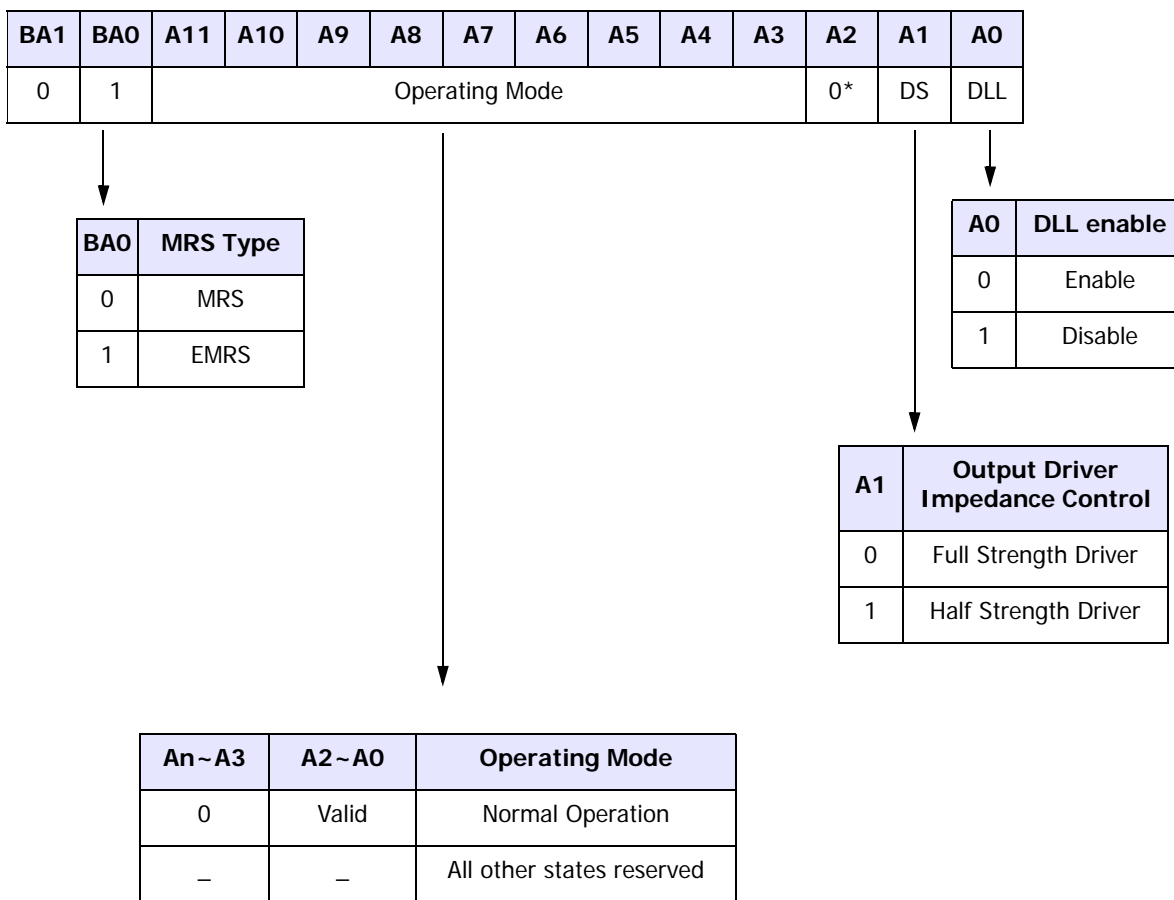
OUTPUT DRIVER IMPEDANCE CONTROL

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Hynix also supports a half strength driver option, intended for lighter load and/or point-to-point environments. Selection of the half strength driver option will reduce the output drive strength by 50% of that of the full strength driver. I-V curves for both the full strength driver and the half strength driver are included in this document.

EXTENDED MODE REGISTER SET (EMRS)

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output driver strength selection(optional). These functions are controlled via the bits shown below. The Extended Mode Register is programmed via the Mode Register Set command (BA0=1 and BA1=0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.



* This part do not support/QFC function, A2 must be programmed to Zero.

