

**128Mb DDR SDRAM  
HY5DU28422ETP  
HY5DU28822ETP  
HY5DU281622ETP**

## Revision History

| Revision No. | History  | Draft Date | Remark |
|--------------|--|------------|--------|
| 0.1          | Defined Target Spec.   | Sep. 2003  |        |
| 0.2          | 1) Changed Title from 128M to 128Mb<br>2) Changed Parameter name from Ambient Temperature to Operating Temperature in ABSOLUTE MAXIMUM RATINGS<br>3) Updated High, Low Current Level of Output Driver Strength in DC OPERATING CONDITIONS<br>4) Corrected 6th note and Added 7th note in DC OPERATING CONDITIONS<br>5) Editorial Changes | Aug. 2004  |        |
| 0.3          | State Diagram modified   | Apr. 2006  |        |



## DESCRIPTION

The Hynix HY5DU28422ETP, HY5DU28822ETP and HY5DU281622ETP are a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

The Hynix 128Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL\_2.

## FEATURES

- VDD, VDDQ = 2.5V +/- 0.2V
- All inputs and outputs are compatible with SSTL\_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- tRAS Lock-out function supported
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable /CAS latency 2 / 2.5 / 3 supported
- Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh supported
- 4096 refresh cycles / 64ms
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Full and Half strength driver option controlled by EMRS
- Lead-free product (ROHS\* Compliant)

\* ROHS (Restriction of Hazardous Substances)

## ORDERING INFORMATION

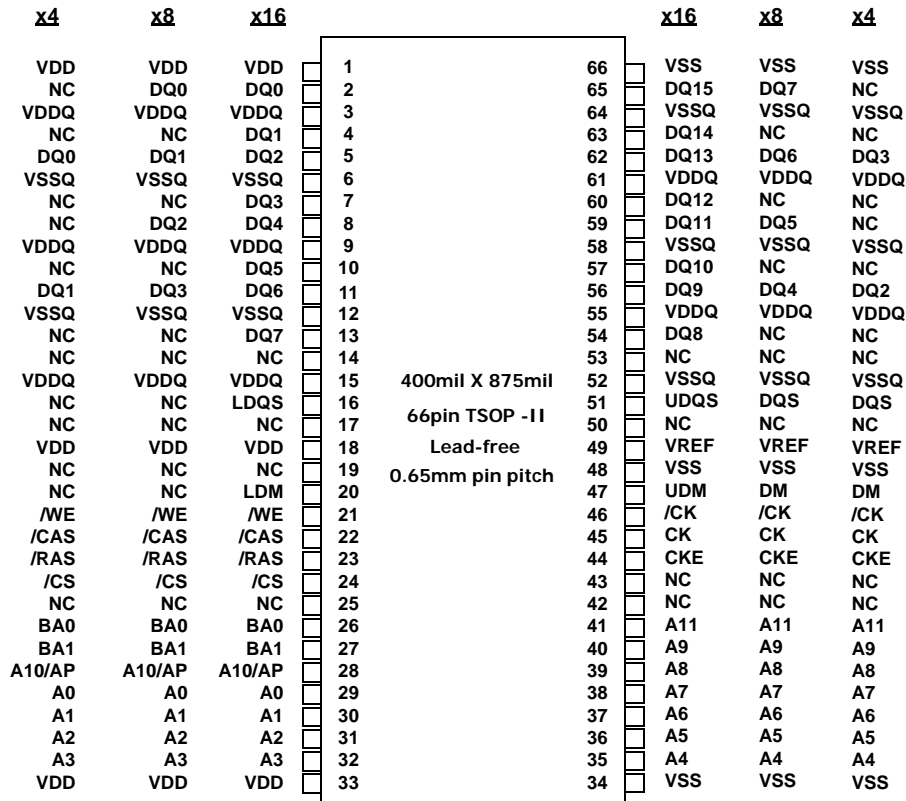
| Part No.          | Configuration | PACKAGE                                |
|-------------------|---------------|--|
| HY5DU28422ETP-X*  | 32Mx4         | 400mil 66pin<br>TSOP-II<br>(Lead-free) |
| HY5DU28822ETP-X*  | 16Mx8         |  |
| HY5DU281622ETP-X* | 8Mx16         |  |

\* X means speed grade

## OPERATING FREQUENCY

| Grade | CL2    | CL2.5  | CL3    | Remark<br>(CL-tRCD-tRP)              |
|-------|--------|--------|--------|--------------------------------------|
| - J   | 133MHz | 166MHz | 166MHz | DDR333 (2.5-3-3) /<br>166MHz (3-3-3) |
| -M    | 133MHz | 133MHz | -      | DDR266 (2-2-2)                       |
| - K   | 133MHz | 133MHz | -      | DDR266A (2-3-3)                      |
| - H   | 100MHz | 133MHz | -      | DDR266B (2.5-3-3)                    |
| - L   | 100MHz | 125MHz | -      | DDR200 (2-2-2)                       |

**PIN CONFIGURATION(TSOP)**



**ROW AND COLUMN ADDRESS TABLE**

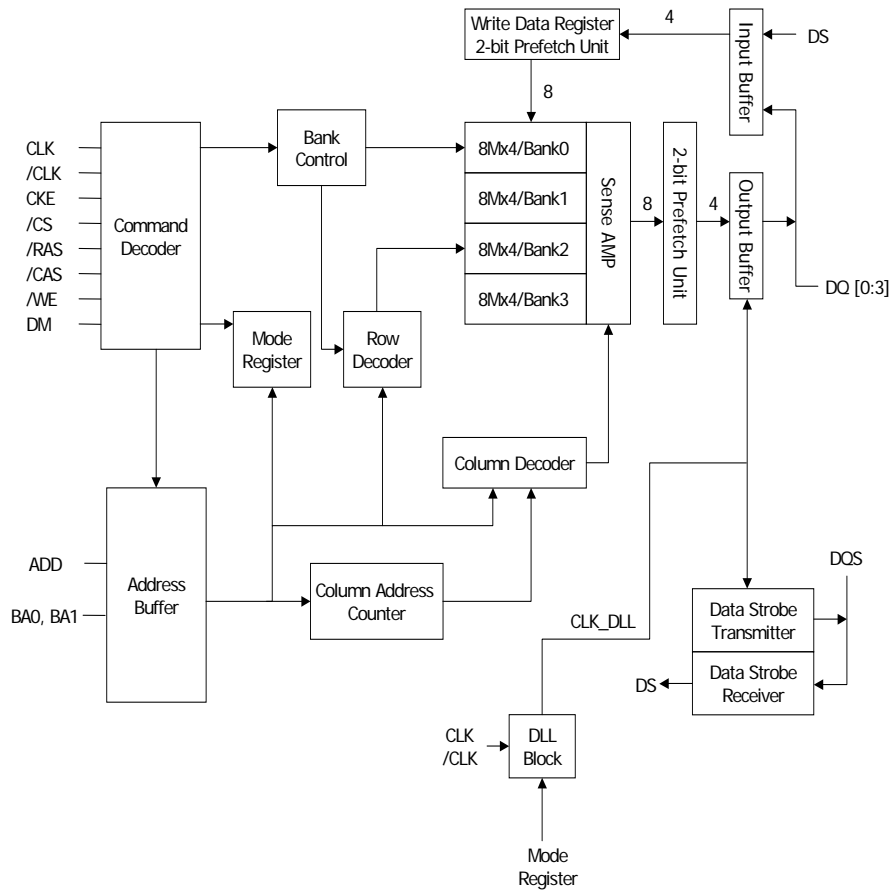
| ITEMS               | 32Mx4           | 16Mx8           | 8Mx16            |
|---------------------|-----------------|-----------------|------------------|
| Organization        | 8M x 4 x 4banks | 4M x 8 x 4banks | 2M x 16 x 4banks |
| Row Address         | A0 - A11        | A0 - A11        | A0 - A11         |
| Column Address      | A0-A9, A11      | A0-A9           | A0-A8            |
| Bank Address        | BA0, BA1        | BA0, BA1        | BA0, BA1         |
| Auto Precharge Flag | A10             | A10             | A10              |
| Refresh             | 4K              | 4K              | 4K               |

## PIN DESCRIPTION

| PIN                 | TYPE   | DESCRIPTION  |
|---------------------|--------|--|
| CK, /CK             | Input  | Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).   |
| CKE                 | Input  | Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. |
| /CS                 | Input  | Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.  |
| BA0, BA1            | Input  | Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.  |
| A0 ~ A11            | Input  | Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).  |
| /RAS, /CAS, /WE     | Input  | Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.  |
| DM<br>(LDM, UDM)    | Input  | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.   |
| DQS<br>(LDQS, UDQS) | I/O    | Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.  |
| DQ                  | I/O    | Data input / output pin: Data bus  |
| VDD/VSS             | Supply | Power supply for internal circuits and input buffers.  |
| VDDQ/VSSQ           | Supply | Power supply for output buffers for noise immunity.  |
| VREF                | Supply | Reference voltage for inputs for SSTL interface.   |
| NC                  | NC     | No connection.   |

## FUNCTIONAL BLOCK DIAGRAM (32Mx4)

4Banks x 8Mbit x 4 I/O Double Data Rate Synchronous DRAM







## SIMPLIFIED COMMAND TRUTH TABLE

| Command                    |       | CKEn-1 | CKEn | CS | RAS | CAS | WE | ADDR    | A10/<br>AP | BA | Note |
|----------------------------|-------|--------|------|----|-----|-----|----|---------|------------|----|------|
| Extended Mode Register Set |       | H      | X    | L  | L   | L   | L  | OP code |            |    | 1,2  |
| Mode Register Set          |       | H      | X    | L  | L   | L   | L  | OP code |            |    | 1,2  |
| Device Deselect            |       | H      | X    | H  | X   | X   | X  | X       |            |    | 1    |
| No Operation               |       |        |      | L  | H   | H   | H  |         |            |    |      |
| Bank Active                |       | H      | X    | L  | L   | H   | H  | RA      |            | V  | 1    |
| Read                       |       | H      | X    | L  | H   | L   | H  | CA      | L          | V  | 1    |
| Read with Autoprecharge    |       |        |      |    |     |     |    |         | H          |    | 1,3  |
| Write                      |       | H      | X    | L  | H   | L   | L  | CA      | L          | V  | 1    |
| Write with Autoprecharge   |       |        |      |    |     |     |    |         | H          |    | 1,4  |
| Precharge All Banks        |       | H      | X    | L  | L   | H   | L  | X       | H          | X  | 1,5  |
| Precharge selected Bank    |       |        |      |    |     |     |    |         | L          | V  | 1    |
| Read Burst Stop            |       | H      | X    | L  | H   | H   | L  | X       |            |    | 1    |
| Auto Refresh               |       | H      | H    | L  | L   | L   | H  | X       |            |    | 1    |
| Self Refresh               | Entry | H      | L    | L  | L   | L   | H  | X       |            |    | 1    |
|                            | Exit  | L      | H    | H  | X   | X   | X  |         |            |    | 1    |
| Precharge Power Down Mode  | Entry |        |      | H  | L   | H   | X  | X       | X          | X  |      |
|                            |       | L      | H    |    |     | H   | H  | 1       |            |    |      |
|                            | Exit  | L      | H    | H  | X   | X   | X  | 1       |            |    |      |
|                            |       |        |      | L  | H   | H   | H  | 1       |            |    |      |
| Active Power Down Mode     | Entry | H      | L    | H  | X   | X   | X  | X       |            |    | 1    |
|                            |       |        |      | L  | V   | V   | V  |         |            |    | 1    |
|                            | Exit  | L      | H    | X  |     |     |    |         |            |    | 1    |

( H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation )

**Note:**

- LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
- OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
- If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
- If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Precharge delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
- If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

## WRITE MASK TRUTH TABLE

| Function     | CKEn-1 | CKEn | /CS, /RAS, /CAS, /WE | DM | ADDR | A10/AP | BA | Note |
|--------------|--------|------|----------------------|----|------|--------|----|------|
| Data Write   | H      | X    | X                    | L  |      | X      |    | 1    |
| Data-In Mask | H      | X    | X                    | H  |      | X      |    | 1    |

**Note:**

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strokes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

### OPERATION COMMAND TRUTH TABLE-I

| Current State | /CS | /RAS | /CAS | /WE | Address    | Command       | Action   |
|---------------|-----|------|------|-----|------------|---------------|--|
| IDLE          | H   | X    | X    | X   | X          | DSEL          | NOP or power down <sup>3</sup>                 |
|               | L   | H    | H    | H   | X          | NOP           | NOP or power down <sup>3</sup>                 |
|               | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>4</sup>                           |
|               | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | ILLEGAL <sup>4</sup>                           |
|               | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | ILLEGAL <sup>4</sup>                           |
|               | L   | L    | H    | H   | BA, RA     | ACT           | Row Activation                                 |
|               | L   | L    | H    | L   | BA, AP     | PRE/PALL      | NOP  |
|               | L   | L    | L    | H   | X          | AREF/SREF     | Auto Refresh or Self Refresh <sup>5</sup>      |
|               | L   | L    | L    | L   | OPCODE     | MRS           | Mode Register Set                              |
| ROW ACTIVE    | H   | X    | X    | X   | X          | DSEL          | NOP  |
|               | L   | H    | H    | H   | X          | NOP           | NOP  |
|               | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>4</sup>                           |
|               | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | Begin read: optional AP <sup>6</sup>           |
|               | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | Begin write: optional AP <sup>6</sup>          |
|               | L   | L    | H    | H   | BA, RA     | ACT           | ILLEGAL <sup>4</sup>                           |
|               | L   | L    | H    | L   | BA, AP     | PRE/PALL      | Precharge <sup>7</sup>                         |
|               | L   | L    | L    | H   | X          | AREF/SREF     | ILLEGAL <sup>11</sup>                          |
|               | L   | L    | L    | L   | OPCODE     | MRS           | ILLEGAL <sup>11</sup>                          |
| READ          | H   | X    | X    | X   | X          | DSEL          | Continue burst to end                          |
|               | L   | H    | H    | H   | X          | NOP           | Continue burst to end                          |
|               | L   | H    | H    | L   | X          | BST           | Terminate burst                                |
|               | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | Term burst, new read: optional AP <sup>8</sup> |
|               | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | ILLEGAL  |
|               | L   | L    | H    | H   | BA, RA     | ACT           | ILLEGAL <sup>4</sup>                           |
|               | L   | L    | H    | L   | BA, AP     | PRE/PALL      | Term burst, precharge                          |
|               | L   | L    | L    | H   | X          | AREF/SREF     | ILLEGAL <sup>11</sup>                          |
|               | L   | L    | L    | L   | OPCODE     | MRS           | ILLEGAL <sup>11</sup>                          |
| WRITE         | H   | X    | X    | X   | X          | DSEL          | Continue burst to end                          |
|               | L   | H    | H    | H   | X          | NOP           | Continue burst to end                          |
|               | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>4</sup>                           |
|               | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | Term burst, new read: optional AP <sup>8</sup> |
|               | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | Term burst, new write: optional AP             |

## OPERATION COMMAND TRUTH TABLE-II

| Current State            | /CS | /RAS | /CAS | /WE    | Address    | Command               | Action                   |
|--------------------------|-----|------|------|--------|------------|-----------------------|--------------------------|
| WRITE                    | L   | L    | H    | H      | BA, RA     | ACT                   | ILLEGAL <sup>4</sup>     |
|                          | L   | L    | H    | L      | BA, AP     | PRE/PALL              | Term burst, precharge    |
|                          | L   | L    | L    | H      | X          | AREF/SREF             | ILLEGAL <sup>11</sup>    |
|                          | L   | L    | L    | L      | OPCODE     | MRS                   | ILLEGAL <sup>11</sup>    |
| READ WITH AUTOPRE-CHARGE | H   | X    | X    | X      | X          | DSEL                  | Continue burst to end    |
|                          | L   | H    | H    | H      | X          | NOP                   | Continue burst to end    |
|                          | L   | H    | H    | L      | X          | BST                   | ILLEGAL                  |
|                          | L   | H    | L    | H      | BA, CA, AP | READ/READAP           | ILLEGAL <sup>10</sup>    |
|                          | L   | H    | L    | L      | BA, CA, AP | WRITE/WRITEAP         | ILLEGAL <sup>10</sup>    |
|                          | L   | L    | H    | H      | BA, RA     | ACT                   | ILLEGAL <sup>4,10</sup>  |
|                          | L   | L    | H    | L      | BA, AP     | PRE/PALL              | ILLEGAL <sup>4,10</sup>  |
|                          | L   | L    | L    | H      | X          | AREF/SREF             | ILLEGAL <sup>11</sup>    |
| WRITE AUTOPRE-CHARGE     | H   | X    | X    | X      | X          | DSEL                  | Continue burst to end    |
|                          | L   | H    | H    | H      | X          | NOP                   | Continue burst to end    |
|                          | L   | H    | H    | L      | X          | BST                   | ILLEGAL                  |
|                          | L   | H    | L    | H      | BA, CA, AP | READ/READAP           | ILLEGAL <sup>10</sup>    |
|                          | L   | H    | L    | L      | BA, CA, AP | WRITE/WRITEAP         | ILLEGAL <sup>10</sup>    |
|                          | L   | L    | H    | H      | BA, RA     | ACT                   | ILLEGAL <sup>4,10</sup>  |
|                          | L   | L    | H    | L      | BA, AP     | PRE/PALL              | ILLEGAL <sup>4,10</sup>  |
|                          | L   | L    | L    | H      | X          | AREF/SREF             | ILLEGAL <sup>11</sup>    |
| PRE-CHARGE               | H   | X    | X    | X      | X          | DSEL                  | NOP-Enter IDLE after tRP |
|                          | L   | H    | H    | H      | X          | NOP                   | NOP-Enter IDLE after tRP |
|                          | L   | H    | H    | L      | X          | BST                   | ILLEGAL <sup>4</sup>     |
|                          | L   | H    | L    | H      | BA, CA, AP | READ/READAP           | ILLEGAL <sup>4,10</sup>  |
|                          | L   | H    | L    | L      | BA, CA, AP | WRITE/WRITEAP         | ILLEGAL <sup>4,10</sup>  |
|                          | L   | L    | H    | H      | BA, RA     | ACT                   | ILLEGAL <sup>4,10</sup>  |
|                          | L   | L    | H    | L      | BA, AP     | PRE/PALL              | NOP-Enter IDLE after tRP |
|                          | L   | L    | L    | H      | X          | AREF/SREF             | ILLEGAL <sup>11</sup>    |
| L                        | L   | L    | L    | OPCODE | MRS        | ILLEGAL <sup>11</sup> |                          |

### OPERATION COMMAND TRUTH TABLE-III

| Current State                        | /CS | /RAS | /CAS | /WE | Address    | Command       | Action                           |
|--------------------------------------|-----|------|------|-----|------------|---------------|----------------------------------|
| ROW ACTIVATING                       | H   | X    | X    | X   | X          | DSEL          | NOP - Enter ROW ACT after tRCD   |
|                                      | L   | H    | H    | H   | X          | NOP           | NOP - Enter ROW ACT after tRCD   |
|                                      | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>4</sup>             |
|                                      | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | ILLEGAL <sup>4,10</sup>          |
|                                      | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | ILLEGAL <sup>4,10</sup>          |
|                                      | L   | L    | H    | H   | BA, RA     | ACT           | ILLEGAL <sup>4,9,10</sup>        |
|                                      | L   | L    | H    | L   | BA, AP     | PRE/PALL      | ILLEGAL <sup>4,10</sup>          |
|                                      | L   | L    | L    | H   | X          | AREF/SREF     | ILLEGAL <sup>11</sup>            |
|                                      | L   | L    | L    | L   | OPCODE     | MRS           | ILLEGAL <sup>11</sup>            |
| WRITE RECOVERING                     | H   | X    | X    | X   | X          | DSEL          | NOP - Enter ROW ACT after tWR    |
|                                      | L   | H    | H    | H   | X          | NOP           | NOP - Enter ROW ACT after tWR    |
|                                      | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>4</sup>             |
|                                      | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | ILLEGAL                          |
|                                      | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | ILLEGAL                          |
|                                      | L   | L    | H    | H   | BA, RA     | ACT           | ILLEGAL <sup>4,10</sup>          |
|                                      | L   | L    | H    | L   | BA, AP     | PRE/PALL      | ILLEGAL <sup>4,11</sup>          |
|                                      | L   | L    | L    | H   | X          | AREF/SREF     | ILLEGAL <sup>11</sup>            |
|                                      | L   | L    | L    | L   | OPCODE     | MRS           | ILLEGAL <sup>11</sup>            |
| WRITE RECOVERING WITH AUTOPRE-CHARGE | H   | X    | X    | X   | X          | DSEL          | NOP - Enter precharge after tDPL |
|                                      | L   | H    | H    | H   | X          | NOP           | NOP - Enter precharge after tDPL |
|                                      | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>4</sup>             |
|                                      | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | ILLEGAL <sup>4,8,10</sup>        |
|                                      | L   | H    | L    | L   | BA, CA, AP | WRITE/WRITEAP | ILLEGAL <sup>4,10</sup>          |
|                                      | L   | L    | H    | H   | BA, RA     | ACT           | ILLEGAL <sup>4,10</sup>          |
|                                      | L   | L    | H    | L   | BA, AP     | PRE/PALL      | ILLEGAL <sup>4,11</sup>          |
|                                      | L   | L    | L    | H   | X          | AREF/SREF     | ILLEGAL <sup>11</sup>            |
|                                      | L   | L    | L    | L   | OPCODE     | MRS           | ILLEGAL <sup>11</sup>            |
| REFRESHING                           | H   | X    | X    | X   | X          | DSEL          | NOP - Enter IDLE after tRC       |
|                                      | L   | H    | H    | H   | X          | NOP           | NOP - Enter IDLE after tRC       |
|                                      | L   | H    | H    | L   | X          | BST           | ILLEGAL <sup>11</sup>            |
|                                      | L   | H    | L    | H   | BA, CA, AP | READ/READAP   | ILLEGAL <sup>11</sup>            |

**OPERATION COMMAND TRUTH TABLE-IV**

| Current State           | /CS | /RAS | /CAS | /WE    | Address    | Command               | Action                      |
|-------------------------|-----|------|------|--------|------------|-----------------------|-----------------------------|
| WRITE                   | L   | H    | L    | L      | BA, CA, AP | WRITE/WRITEAP         | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | H    | H      | BA, RA     | ACT                   | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | H    | L      | BA, AP     | PRE/PALL              | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | L    | H      | X          | AREF/SREF             | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | L    | L      | OPCODE     | MRS                   | ILLEGAL <sup>11</sup>       |
| MODE REGISTER ACCESSING | H   | X    | X    | X      | X          | DSEL                  | NOP - Enter IDLE after tMRD |
|                         | L   | H    | H    | H      | X          | NOP                   | NOP - Enter IDLE after tMRD |
|                         | L   | H    | H    | L      | X          | BST                   | ILLEGAL <sup>11</sup>       |
|                         | L   | H    | L    | H      | BA, CA, AP | READ/READAP           | ILLEGAL <sup>11</sup>       |
|                         | L   | H    | L    | L      | BA, CA, AP | WRITE/WRITEAP         | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | H    | H      | BA, RA     | ACT                   | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | H    | L      | BA, AP     | PRE/PALL              | ILLEGAL <sup>11</sup>       |
|                         | L   | L    | L    | H      | X          | AREF/SREF             | ILLEGAL <sup>11</sup>       |
| L                       | L   | L    | L    | OPCODE | MRS        | ILLEGAL <sup>11</sup> |                             |

**Note:**

1. H - Logic High Level, L - Logic Low Level, X - Don't Care, V - Valid Data Input, BA - Bank Address, AP - AutoPrecharge Address, CA - Column Address, RA - Row Address, NOP - NO Operation.
2. All entries assume that CKE was active(high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive(low level), then in power down mode.
4. Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA) depending on the state of that bank.
5. If both banks are idle and CKE is inactive(low level), then self refresh mode.
6. Illegal if tRCD is not met.
7. Illegal if tRAS is not met.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Illegal if tRRD is not met.
10. Illegal for single bank, but legal for other banks in multi-bank devices.
11. Illegal for all banks.

### CKE FUNCTION TRUTH TABLE

| Current State               | CKEn-1 | CKEn | /CS | /RAS | /CAS | /WE | /ADD | Action                                    |
|-----------------------------|--------|------|-----|------|------|-----|------|---|
| SELF REFRESH <sup>1</sup>   | H      | X    | X   | X    | X    | X   | X    | INVALID                                   |
|                             | L      | H    | H   | X    | X    | X   | X    | Exit self refresh, enter idle after tSREX |
|                             | L      | H    | L   | H    | H    | H   | X    | Exit self refresh, enter idle after tSREX |
|                             | L      | H    | L   | H    | H    | L   | X    | ILLEGAL                                   |
|                             | L      | H    | L   | H    | L    | X   | X    | ILLEGAL                                   |
|                             | L      | H    | L   | L    | X    | X   | X    | ILLEGAL                                   |
|                             | L      | L    | X   | X    | X    | X   | X    | NOP, continue self refresh                |
| POWER DOWN <sup>2</sup>     | H      | X    | X   | X    | X    | X   | X    | INVALID                                   |
|                             | L      | H    | H   | X    | X    | X   | X    | Exit power down, enter idle               |
|                             | L      | H    | L   | H    | H    | H   | X    | Exit power down, enter idle               |
|                             | L      | H    | L   | H    | H    | L   | X    | ILLEGAL                                   |
|                             | L      | H    | L   | H    | L    | X   | X    | ILLEGAL                                   |
|                             | L      | H    | L   | L    | X    | X   | X    | ILLEGAL                                   |
|                             | L      | L    | X   | X    | X    | X   | X    | NOP, continue power down mode             |
| ALL BANKS IDLE <sup>4</sup> | H      | H    | X   | X    | X    | X   | X    | See operation command truth table         |
|                             | H      | L    | L   | L    | L    | H   | X    | Enter self refresh                        |
|                             | H      | L    | H   | X    | X    | X   | X    | Exit power down                           |
|                             | H      | L    | L   | H    | H    | H   | X    | Exit power down                           |
|                             | H      | L    | L   | H    | H    | L   | X    | ILLEGAL                                   |
|                             | H      | L    | L   | H    | L    | X   | X    | ILLEGAL                                   |
|                             | H      | L    | L   | L    | H    | X   | X    | ILLEGAL                                   |
|                             | H      | L    | L   | L    | L    | L   | X    | ILLEGAL                                   |
|                             | L      | L    | X   | X    | X    | X   | X    | NOP                                       |
| ANY STATE OTHER THAN ABOVE  | H      | H    | X   | X    | X    | X   | X    | See operation command truth table         |
|                             | H      | L    | X   | X    | X    | X   | X    | ILLEGAL <sup>5</sup>                      |
|                             | L      | H    | X   | X    | X    | X   | X    | INVALID                                   |
|                             | L      | L    | X   | X    | X    | X   | X    | INVALID                                   |

**Note:**

When CKE=L, all DQ and DQS must be in Hi-Z state.

1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing any command.
2. All command can be stored after 2 clocks from low to high transition of CKE.
3. Illegal if CLK is suspended or stopped during the power down mode.
4. Self refresh can be entered only from the all banks idle state.
5. Disabling CLK may cause malfunction of any bank which is in active state.







































