

**256Mb DDR SDRAM**  
**HY5DU56422D(L)FP**  
**HY5DU56822D(L)FP**  
**HY5DU561622D(L)FP**

## Revision History

Revision No.	History	Draft Date	Remark
1.0	First Version Release	Mar. 2005	
1.1	State Diagram modified	Apr. 2006	

## DESCRIPTION

The HY5DU56422D(L)FP, HY5DU56822D(L)FP, and HY5DU561622D(L)FP are a 268,435,456-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

This Hynix 256Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL\_2.

## FEATURES

- VDD, VDDQ = 2.5V ± 0.2V for DDR200, 266, 333  
VDD, VDDQ = 2.6V ± 0.1V for DDR400
- All inputs and outputs are compatible with SSTL\_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has two byte-wide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ)  
Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 2/2.5 (DDR200, 266, 333) and 3 (DDR400) supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh supported
- tRAS lock out function supported
- 8192 refresh cycles / 64ms
- 60 Ball FBGA Package Type
- Full and Half strength driver option controlled by EMRS
- Lead free (\*ROHS Compliant)

## ORDERING INFORMATION

Part No.	Configuration	Package
HY5DU56422D(L)F-X*	64M x 4	60 Ball FBGA (Lead free)
HY5DU56822D(L)F-X*	32M x 8	
HY5DU561622D(L)F-X*	16M x 16	

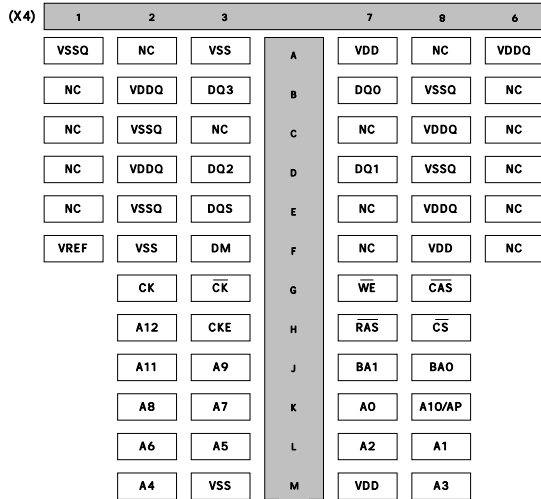
\*X means speed grade

\*ROHS (Restriction Of Hazardous Substances)

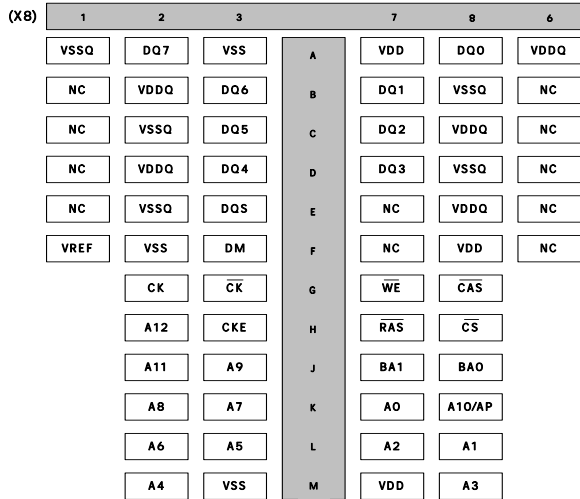
## OPERATING FREQUENCY

Grade	Clock Rate		Remark (CL-tRCD-tRP)
-D43	200MHz@CL3		DDR400B (3-3-3)
- J	133MHz@CL2	166MHz@CL2.5	DDR333 (2.5-3-3)
- K	133MHz@CL2	133MHz@CL2.5	DDR266A (2-3-3)
- H	100MHz@CL2	133MHz@CL2.5	DDR266B (2.5-3-3)
- L	100MHz@CL2		DDR200 (2-2-2)

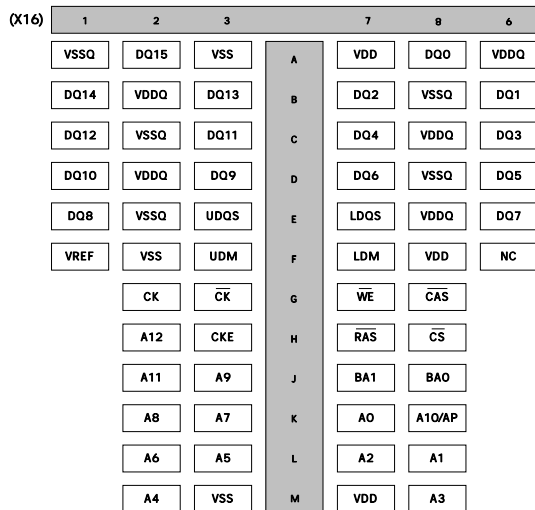
## PIN CONFIGURATION



x4 Device Ball Pattern



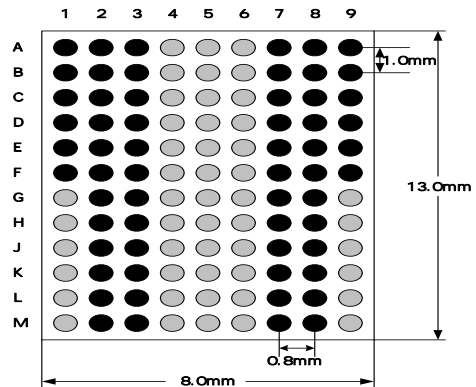
x8 Device Ball Pattern



x16 Device Ball Pattern

- : Ball Existing [ For Reference Only ]
- : Depopulated Ball

Top View (See the balls through the Package)



BGA Package Ball Pattern Top View

## ROW AND COLUMN ADDRESS TABLE

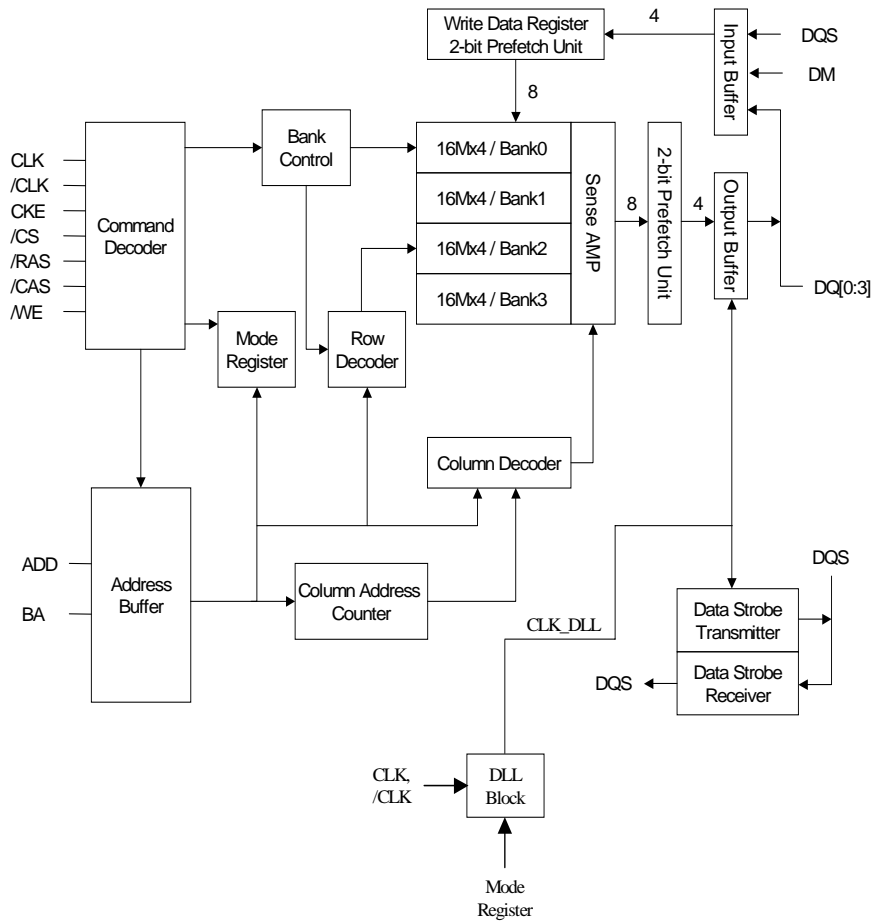
ITEMS	64Mx4	32Mx8	16Mx16
Organization	16M x 4 x 4banks	8M x 8 x 4banks	4M x 16 x 4banks
Row Address	A0 - A12	A0 - A12	A0 - A12
Column Address	A0-A9, A11	A0-A9	A0-A8
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto Precharge Flag	A10	A10	A10
Refresh	8K	8K	8K

## PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied.
/CS	Input	Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin: Data bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

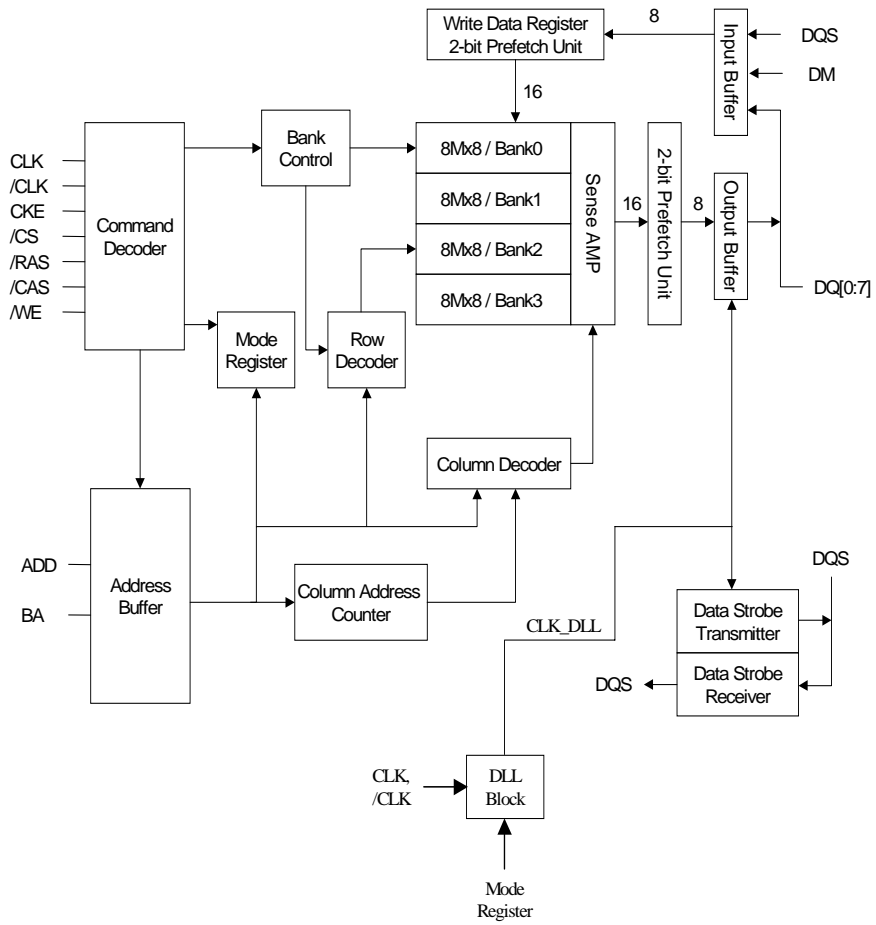
## FUNCTIONAL BLOCK DIAGRAM (64Mx4)

4Banks x 16Mbit x 4 I/O Double Data Rate Synchronous DRAM



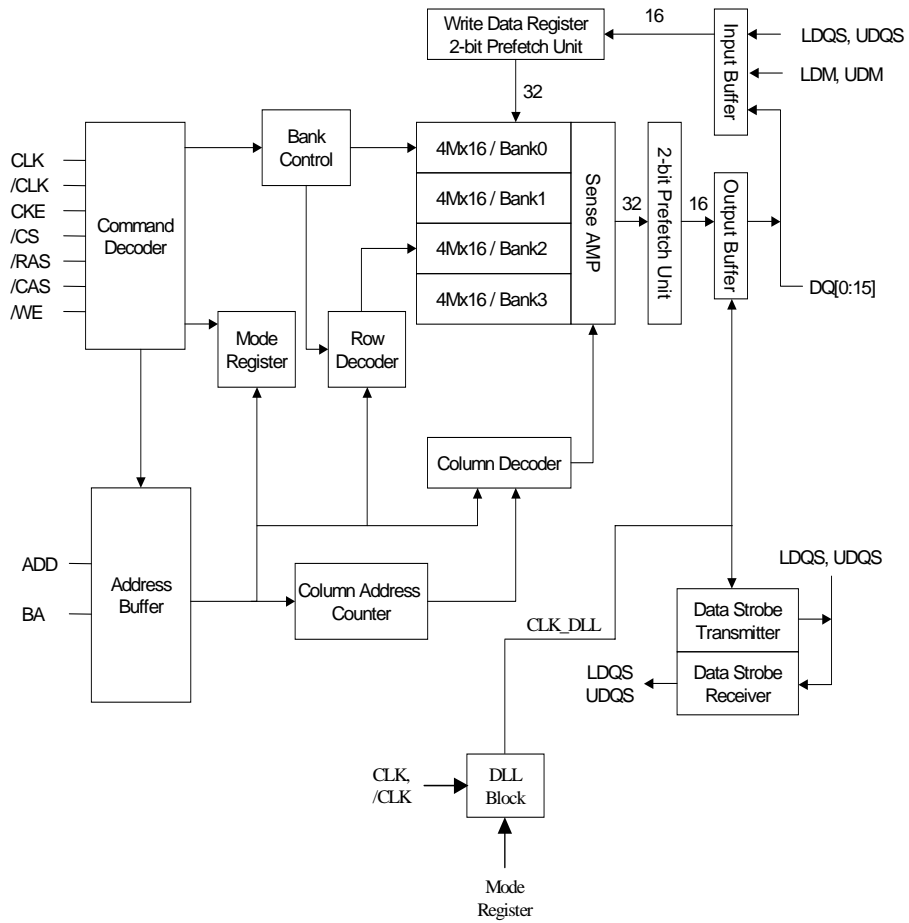
## FUNCTIONAL BLOCK DIAGRAM (32Mx8)

4Banks x 8Mbit x 8 I/O Double Data Rate Synchronous DRAM



## FUNCTIONAL BLOCK DIAGRAM (16Mx16)

4Banks x 4Mbit x 16 I/O Double Data Rate Synchronous DRAM



## SIMPLIFIED COMMAND TRUTH TABLE

Command	CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA
Extended Mode Register Set <sup>1,2</sup>	H	X	L	L	L	L	OP code		
Mode Register Set <sup>1,2</sup>	H	X	L	L	L	L	OP code		
Device Deselect <sup>1</sup>	H	X	H	X	X	X	X		
No Operation <sup>1</sup>			L	H	H	H			
Bank Active <sup>1</sup>	H	X	L	L	H	H	RA		V
Read <sup>1</sup>	H	X	L	H	L	H	CA	L	V
Read with Autoprecharge <sup>1,3</sup>								H	
Write <sup>1</sup>	H	X	L	H	L	L	CA	L	V
Write with Autoprecharge <sup>1,4</sup>								H	
Precharge All Banks <sup>1,5</sup>	H	X	L	L	H	L	X	H	X
Precharge selected Bank <sup>1</sup>								L	V
Read Burst Stop <sup>1</sup>	H	X	L	H	H	L	X		
Auto Refresh <sup>1</sup>	H	H	L	L	L	H	X		
Self Refresh <sup>1</sup>	Entry	H	L	L	L	L	H	X	
	Exit	L	H	H	X	X	X		
Precharge Power Down Mode <sup>1</sup>	Entry	H	L	H	X	X	X	X	
				L	H	H	H		
	Exit	L	H	H	X	X	X		
				L	H	H	H		
Active Power Down Mode <sup>1</sup>	Entry	H	L	H	X	X	X	X	
				L	V	V	V		
	Exit	L	H	X					

( H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation )

**Note:**

1. LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A12 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tWR+tRP). Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

\*For more information about Truth Table, refer to "Device Operation" section in hynix website.

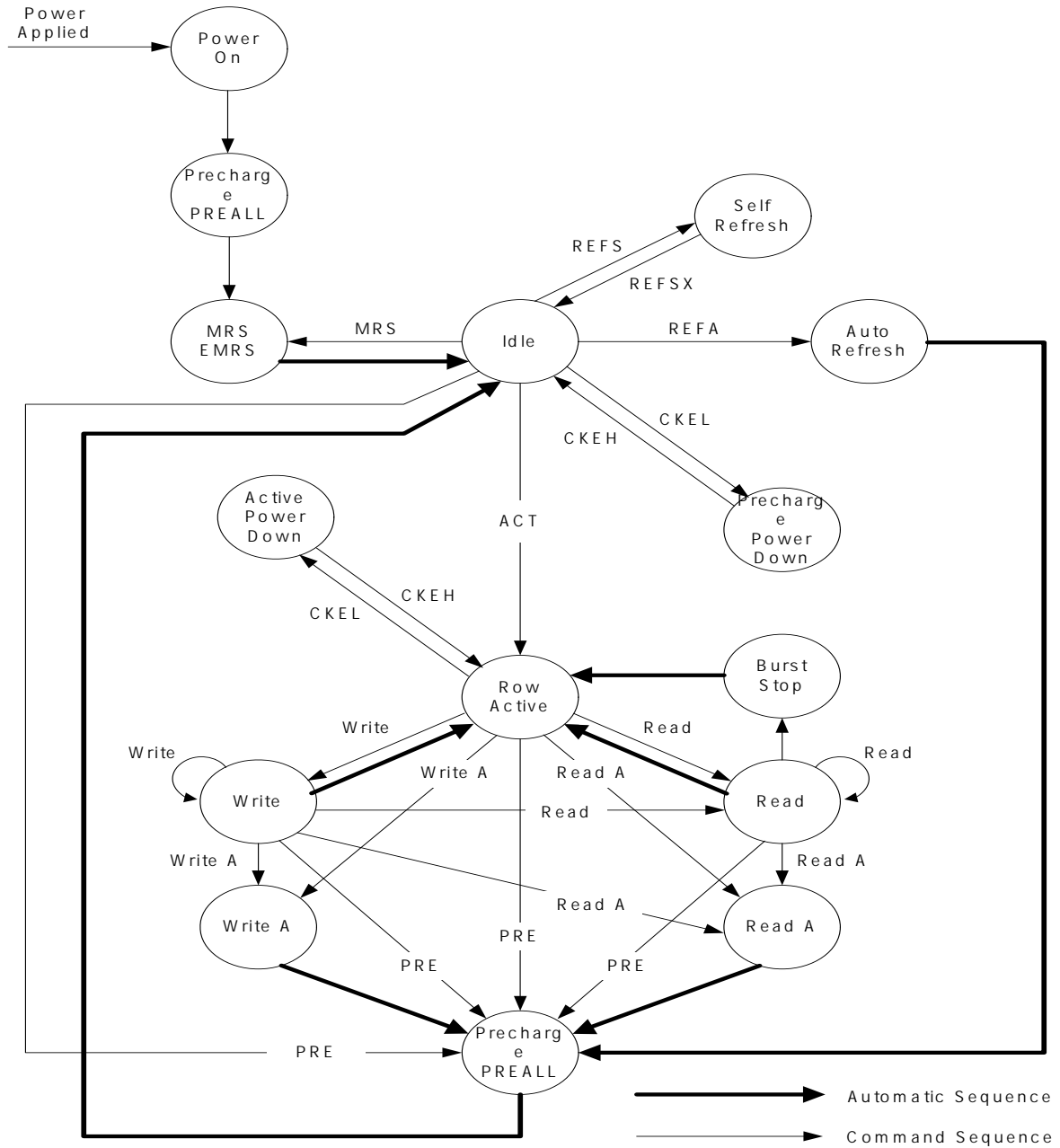
## WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADDR	A10/ AP	BA
Data Write <sup>1</sup>	H	X	X	L		X	
Data-In Mask <sup>1</sup>	H	X	X	H		X	

**Note:**

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strokes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

### SIMPLIFIED STATE DIAGRAM



PREALL = Precharge All Banks  
 MRS = Mode Register Set  
 EMRS = Extended Mode Register Set  
 REFS = Enter Self Refresh  
 REFSX = Exit Self Refresh  
 REFA = Auto Refresh

CKEL = Enter Power Down  
 CKEH = Exit Power Down  
 ACT = Active  
 Write A = Write with Autoprecharge  
 Read A = Read with Autoprecharge  
 PRE = Precharge

## POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied anytime after VDDQ, but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL\_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. After the DLL reset, tXSRD(DLL locking time) should be satisfied for read command. After the Mode Register set command, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated low (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.)
  - VDD and VDDQ are driven from a single power converter output.
  - VTT is limited to  $1.44V$  (reflecting  $VDDQ(max)/2 + 50mV$  VREF variation +  $40mV$  VTT variation).
  - VREF tracks  $VDDQ/2$ .
  - A minimum resistance of 42 Ohms (22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.
  - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	$< VDD + 0.3V$
VTT	After or with VDDQ	$< VDDQ + 0.3V$
VREF	After or with VDDQ	$< VDDQ + 0.3V$

2. Start clock and maintain stable clock for a minimum of 200usec.
3. After stable power and clock, apply NOP condition and take CKE high.
4. Issue Extended Mode Register Set (EMRS) to enable DLL.
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=high. (An additional 200 cycles(tXSRD) of clock are required for locking DLL)
6. Issue Precharge commands for all banks of the device.
7. Issue 2 or more Auto Refresh commands.
8. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low





































