256Mb(16Mx16) DDR2 SDRAM

HY5PS561621AFP

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Graphics Version Release	Jan. 2005	
0.2	300Mhz Speed Bin & Lead Free Comment Insert	Mar. 2005	
0.3	AC parameter value change	Mar. 2005	
0.4	AC parameter value change (tRRD, tDQSQ...)	Apr. 2005	
0.5	tCCD Change (for 450MHz)	Aug. 2005	
1.0	IDD Value Insert & VDD/VDDQ max range change	Aug. 2005	
1.1	CAS Latency Value insert at AC timing table	Jan. 2006	
1.2	tWR(500MHz) change from 15ns to 14ns (Page 71)	Jun. 2006	

Note) The HY5PS561621AFP data sheet follows all of JEDEC DDR2 standard.

Contents

1. Description

1.1 Device Features & Ordering Information

1.1.1 Key Features

- VDD/VDDQ=2.0V +/- 0.1V(500/450MHz)
- 1.8V VDD/VDDQ wide range max power supply supports(400/350/300MHz)
- All inputs and outputs are compatible with SSTL_18 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface:two data transfers per clock cycle(tCK)
- Source synchronous-data transaction aligned to bidirectional data strobe (DQS, $\overline{DQS}$)
- Differential Data Strobe (DQS, $\overline{DQS}$)
- Data outputs on DQS, $\overline{DQS}$ edges when read (edged DQ)
- Data inputs on DQS centers when write(centered DQ)
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 4, 5, 6 and 7 supported
- Programmable additive latency 0, 1, 2, 3, 4, 5 supported
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- tRAS lockout supported
- 8K refresh cycles /64ms
- JEDEC standard 84ball FBGA(x16)
- Full strength driver option controlled by EMRS
- On Die Termination supported
- Off Chip Driver Impedance Adjustment supported
- Partial Array Self Refresh supported
- High Temperature Self Refresh rate supported

1.1.2 Ordering Information

Part No.	Power Supply	Clock Frequency	Max Data Rate	Interface	Package
HY5PS561621AFP-2	VDD/VDDQ=2.0V	500MHz	1000Mbps/pin	SSTL_18	84Ball FBGA
HY5PS561621AFP-22		450MHz	900Mbps/pin		
HY5PS561621AFP-25	VDD/VDDQ=1.8V	400MHz	800Mbps/pin		
HY5PS561621AFP-28		350MHz	700Mbps/pin		
HY5PS561621AFP-33		300MHz	600Mbps/pin		

Note)

Hynix supports Lead free parts for each speed grade with same specification, except Lead free materials.

We'll add "P" character after "F" for Lead free product.

For example, the part number of 300MHz Lead free product is HY5PS561621AFP-33.

1.2 16Mx16 DDR2 Pin Configuration

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{UDQS}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{LDQS}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{WE}$	K	$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1	L	$\overline{CAS}$	$\overline{CS}$	
	A10	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

ROW AND COLUMN ADDRESS TABLE

ITEMS	16Mx16
# of Bank	4
Bank Address	BA0, BA1
Auto Precharge Flag	A10/AP
Row Address	A0 - A12
Column Address	A0-A8
Page size	1 KB

1.3 PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry and exit.. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{\text{CK}}$,CKE and ODT are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_18 input, but will detect an LVCMOS LOW level after Vdd is applied.
$\overline{\text{CS}}$	Input	Chip Select : Enables or disables all inputs except CK, $\overline{\text{CK}}$, CKE, DQS and DM. All commands are masked when $\overline{\text{CS}}$ is registered high. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	On Die Termination Control : ODT enables on die termination resistance internal to the DDR2 SDRAM. When enabled, on die termination is only applied to DQ, LDQS, /LDQS, UDQS, /UDQS, LDM and UDM
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
LDM, UDM	Input	Input Data Mask : DM is an input mask signal for write data. Input Data is masked when DM is sampled High coincident with that input data during a WRITE access. DM is sampled on both edges of DQS, Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 ~ A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during MODE REGISTER SET commands.
DQ	Input/Output	Data input / output : Bi-directional data bus
(UDQS),($\overline{\text{UDQS}}$) (LDQS),($\overline{\text{LDQS}}$)	Input/Output	Data Strobe : Output with read data, input with write data. Edge aligned with read data, centered in write data. For the x16, LDQS correspond to the data on DQ0~DQ7; UDQS corresponds to the data on DQ8~DQ15. The data strobes LDQS, UDQS may be used in single ended mode or paired with optional complementary signals $\overline{\text{LDQS}}$, $\overline{\text{UDQS}}$ to provide differential pair signaling to the system during both reads and wirtes. An EMRS(1) control bit enables or disables all complementary data strobe signals.
NC		No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Ground
VDDL	Supply	DLL Power Supply
VSSDL	Supply	DLL Ground
VDD	Supply	Power Supply
VSS	Supply	Ground
VREF	Supply	Reference voltage for inputs for SSTL interface.

In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1)

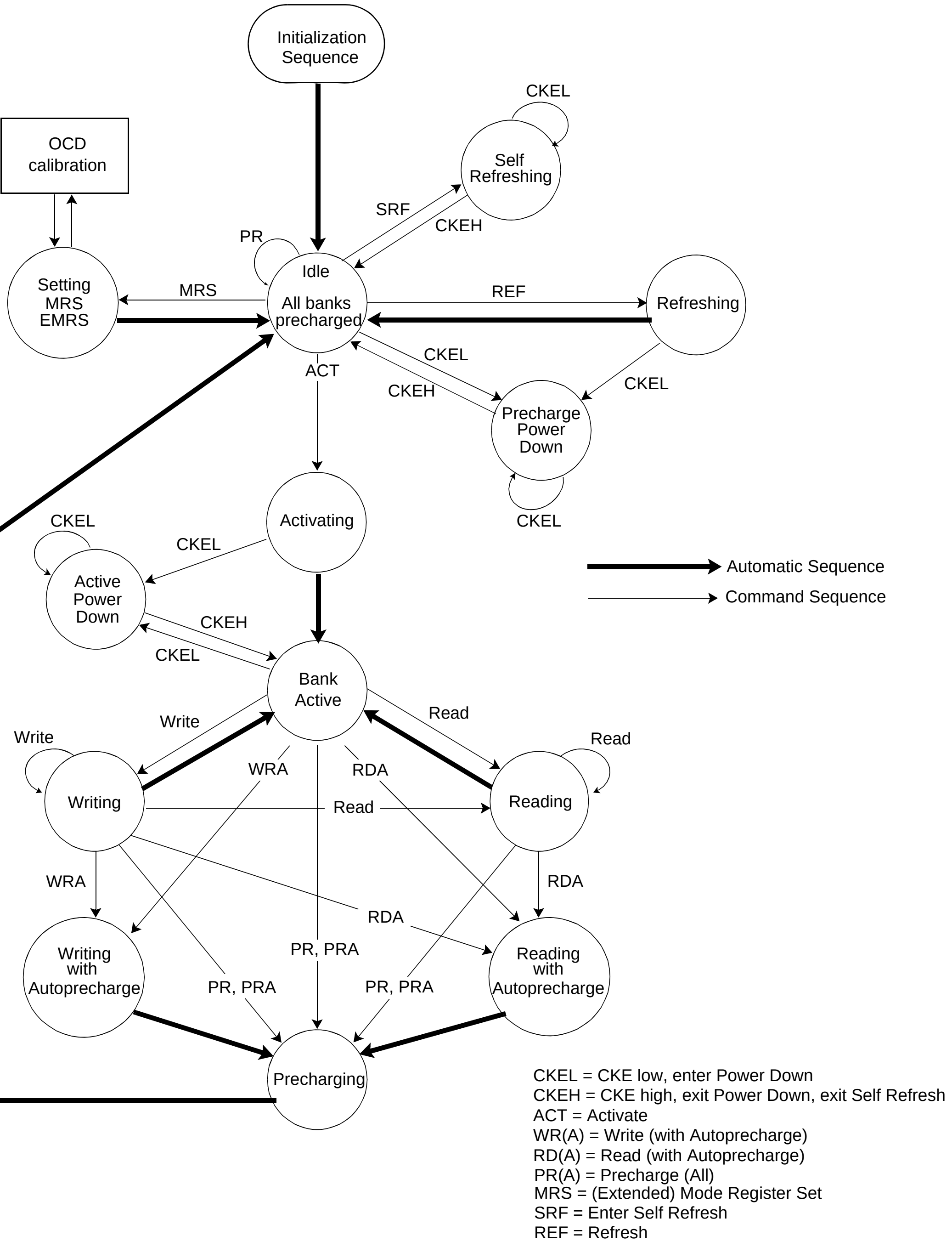
x16 LDQS/$\overline{\text{LDQS}}$ and UDQS/$\overline{\text{UDQS}}$

"single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1)

x16 LDQS and UDQS

2. Functional Description

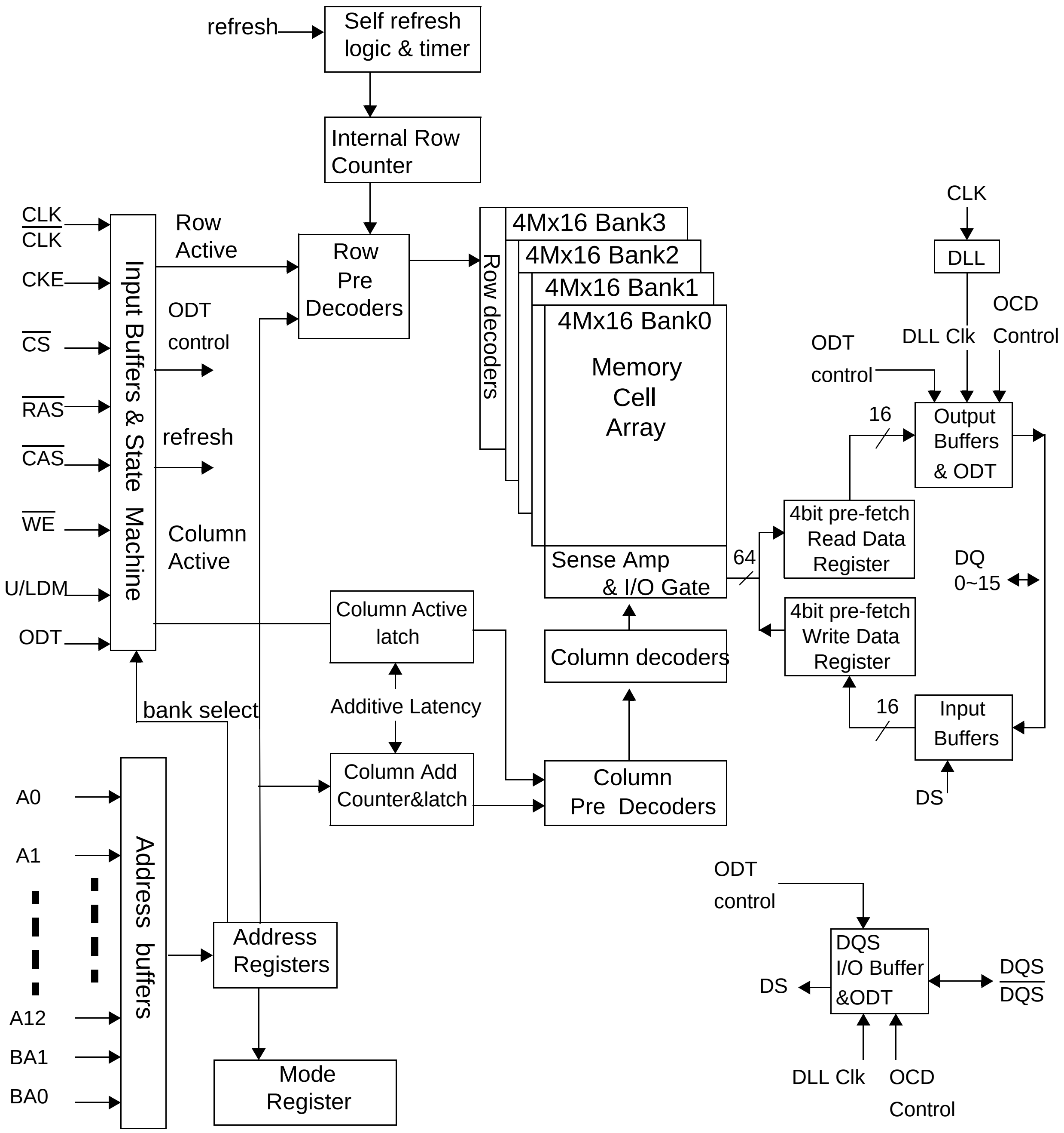
2.1 Simplified State Diagram



Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down enty/exit - among other things - are not captured in full detail.

2.2 Functional Block Diagram (16Mx16)

4Banks x 4Mbit x 16 I/O DDR2 SDRAM



2.3 Basic Function & Operation of DDR2 SDRAM

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.3.1 Power up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200 us after stable power and clock(CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “Low” to BA0, “High” to BA1.)[*2]
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “High” to BA0 and BA1.)[*2]
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1.)
8. Issue a Mode Register Set command for “DLL reset”.
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-1.)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment).
    If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of

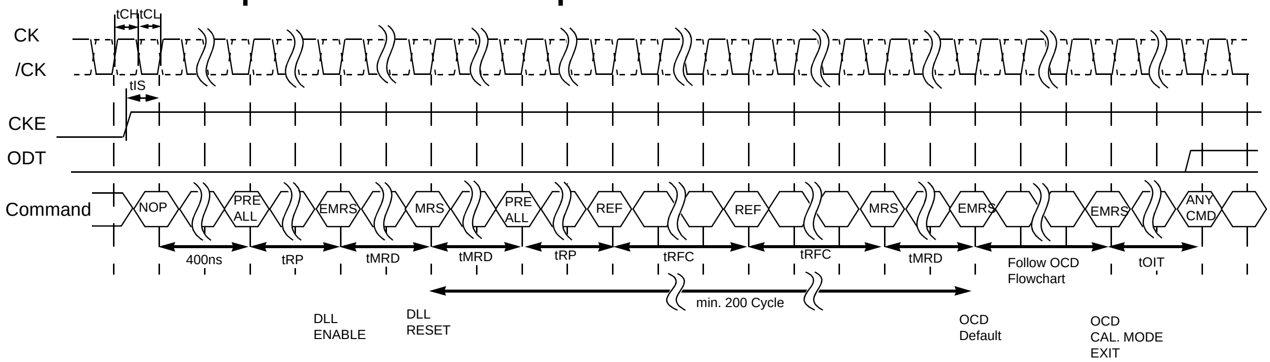
EMRS.

13. The DDR2 SDRAM is now ready for normal operation.

*1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

*2) Sequence 5 and 6 may be performed between 8 and 9.

Initialization Sequence after Power Up



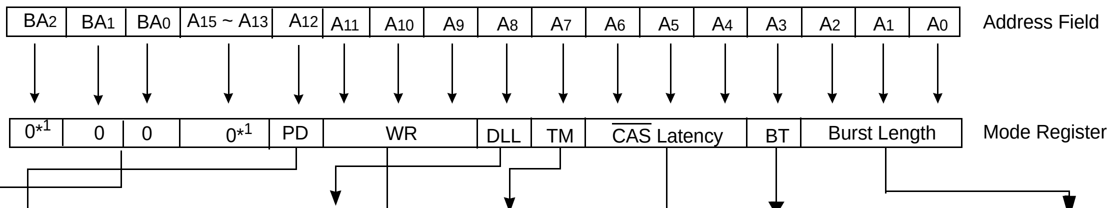
2.3.2 Programming the Mode and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{CAS}$ latency, DLL reset function, write recovery time(tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT(On Die Termination), single-ended strobe, and OCD(off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register(MR) or Extended Mode Registers(EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.3.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to the table for specific codes.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit(use tXARD)
1	Slow exit(use tXARDS)

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)*2
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	Reserved

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	5
1	1	0	6
1	1	1	7

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

*1: BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register. BA2 and A13~A15 are not used for 256Mb

*2: WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

2.3.2.2 DDR2 SDRAM Extended Mode Register Set

EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be written after power-up for proper operation. The extended mode register(1) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1, while controlling the states of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3~A5 determines the additive latency, A7~A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable. A2 and A6 are used for ODT setting.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

EMRS(1) Programming

Address Field	BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Extended Mode Register	0*1	0	1	0*1	0	0	$\overline{DQS}$	OCD program			Rtt	Additive latency			Rtt	D.I.C	DLL

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[a]
1	1	1	OCD Calibration default [b]

a: When Adjust mode is issued, AL from previously set value must be applied.
b: After setting to default, OCD mode needs to be exited by setting A9-A7 to 000. Refer to the following 2.2.2.3 section for detailed information

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff (Optional)[a]
0	Output buffer enabled
1	Output buffer disabled

a. Outputs disabled - DQs, DQSs, $\overline{DQSs}$. This feature is used in conjunction with DIMM IDD meaurements when IDDQ is not desired to be included.

A1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

A10	$\overline{DQS}$
0	Enable
1	Disable

*1 : BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

EMRS(2)

The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be written after power-up for proper operation. The extended mode register(2) is written by asserting low on /CS,/RAS,/CAS,/WE, high on BA1 and low on BA0, while controling the states of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all bank are in the precharge state.

EMRS(2) Programming:

Address Field	BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Extended Mode Register(2)	0*1	1	0	0*1						SRF	0*1				PASR		

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3):Reserved

A7	Hign Temp Self-refresh Rate Enable
1	Enable
0	Disable

A2	A1	A0	Bank Refresh @ PASR
0	0	0	All Bank
0	0	1	Half Array (BA[1:0] = 00 & 01)
0	1	0	Quarter Array (BA[1:0] = 00)
0	1	1	Not defined
1	0	0	3/4 Quarter Array (BA[1:0] = 01, 10 & 11)
1	0	1	Half Array (BA[1:0] = 10 & 11)
1	1	0	Quarter Array (BA[1:0] = 11)
1	1	1	Not defined

*1 : The rest bits in EMRS(2) is reserved for future use and all bits except A7, BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Due to the migration natural, user needs to ensure the DRAM part supports higher than 85 Tcase temperature self-refresh entry. JEDEC standard DDR2 SDRAM Module user can look at DDR2 SDRAM Module SPD fileld Byte 49 bit[0]. If the high temperature self-refresh mode is supported then controller can set the EMRS2 [A7] bit to enable the self-refresh rate in case of higher than 85 temperature self-refresh operation. For the lose part user, please refer to the Hynix web site(www.hynix.com) to check the high temperature self-refresh rate availability. In order to save power consumption, DDR2 DRAM has Partial Array Self Refresh (PASR) option. PASR includes 6 kinds of self refresh mode.

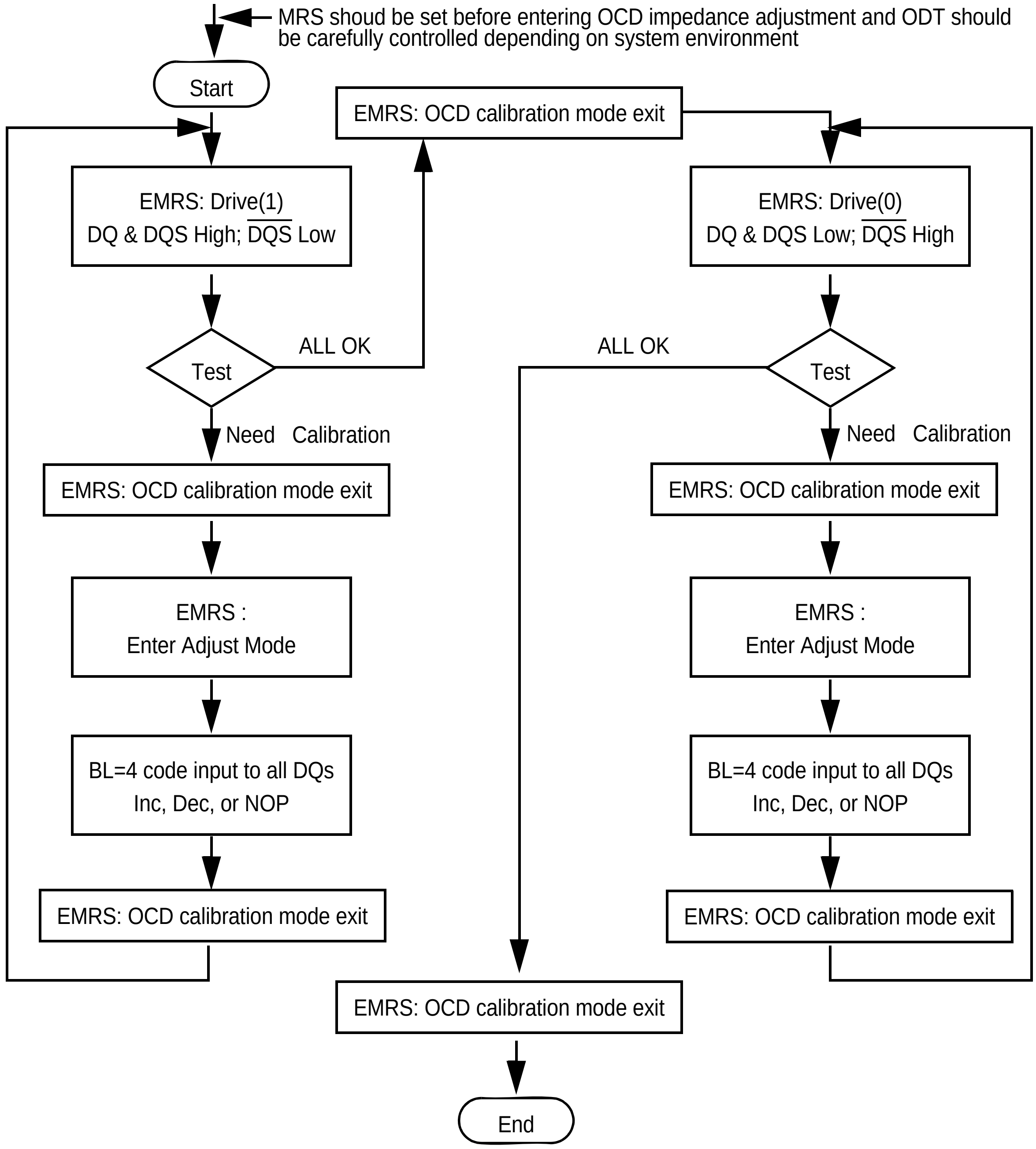
EMRS(3) Programming: Reserved*1

Address Field	BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Extended Mode Register(3)	0*1	1	1	0*1													

*1 : EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

2.3.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termiantion) should be carefully controlled depending on system environment.



Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is depedent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{\text{DQS}}$ signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{\text{DQS}}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Table x. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default output driver

characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Off- Chip-Driver program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{\text{DQS}}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{\text{DQS}}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD impedance adjust

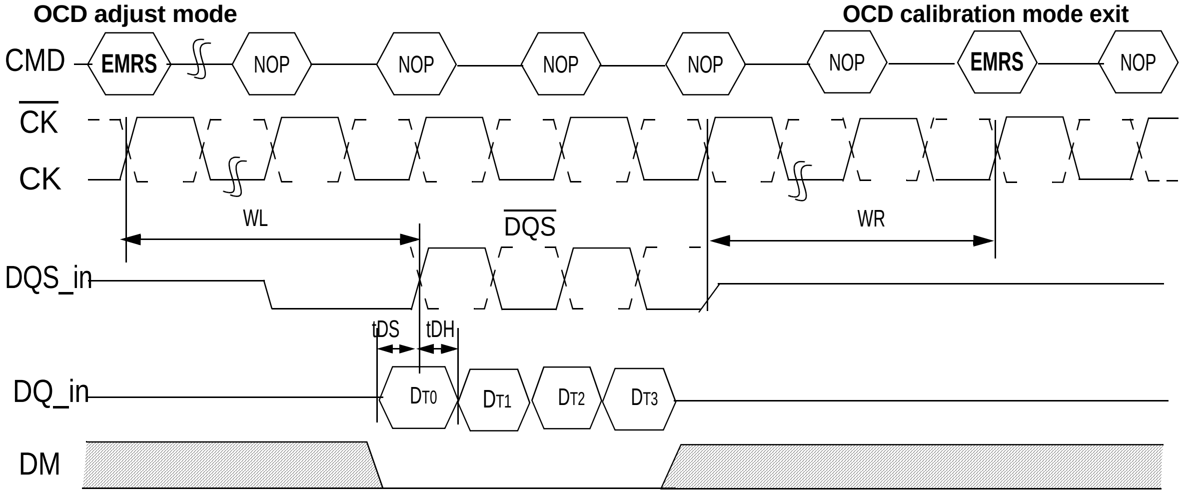
To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in table X. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table X means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied

Table X : Off- Chip-Driver Program

4bit burst code inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step

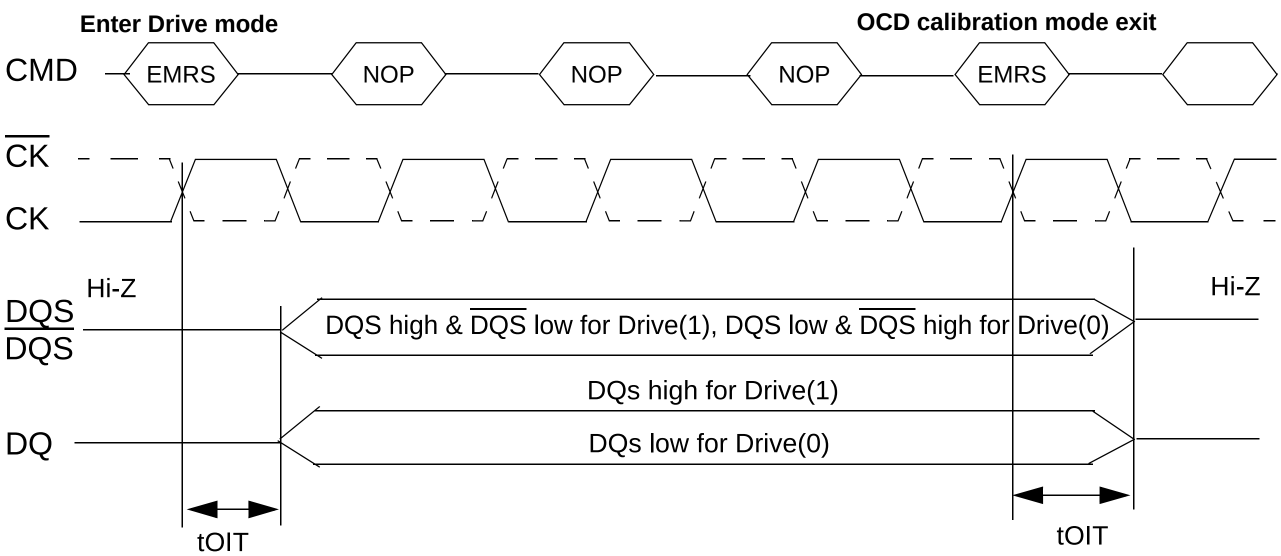
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as the following timing diagram. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by
MRS addressing mode (ie. sequential or interleave).



Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after "enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as the following timing diagram.

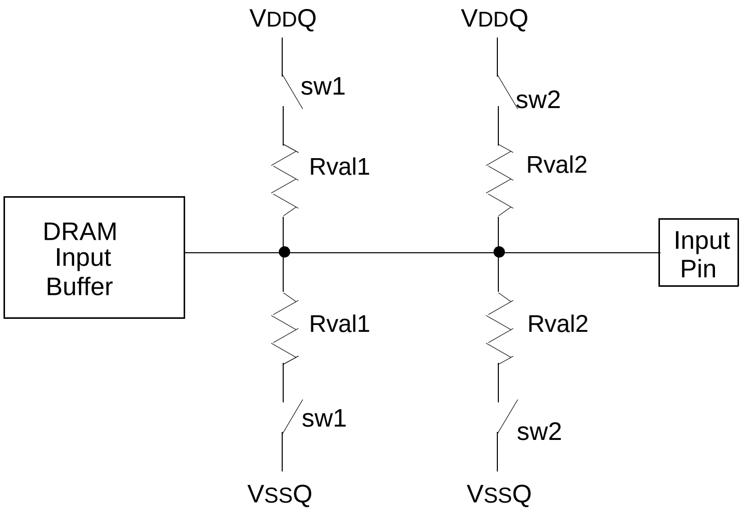


2.3.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

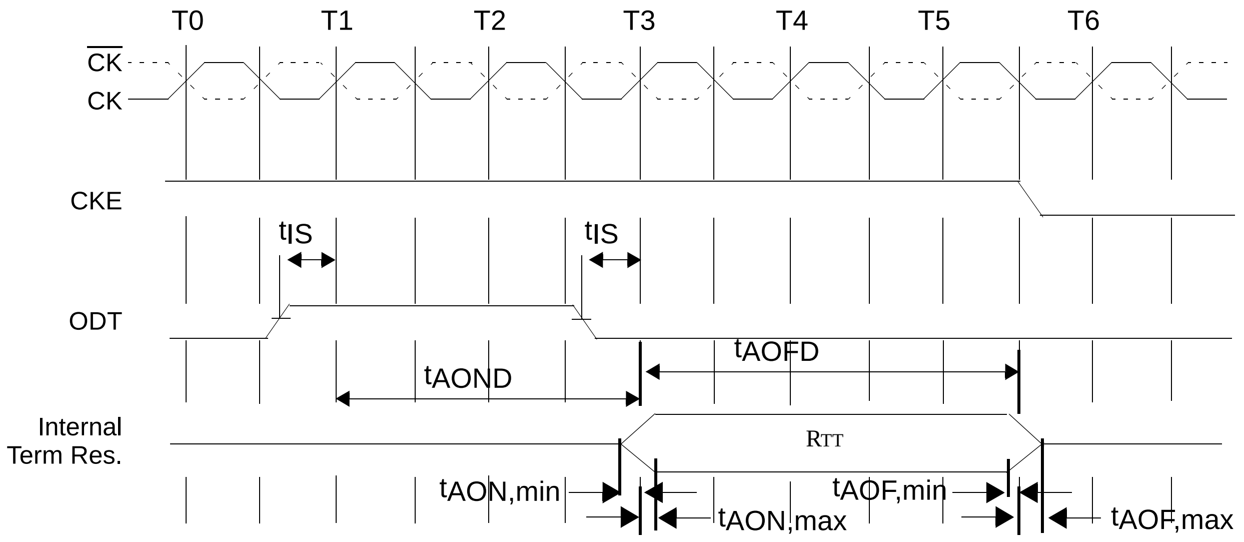
The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.

FUNCTIONAL REPRESENTATION OF ODT

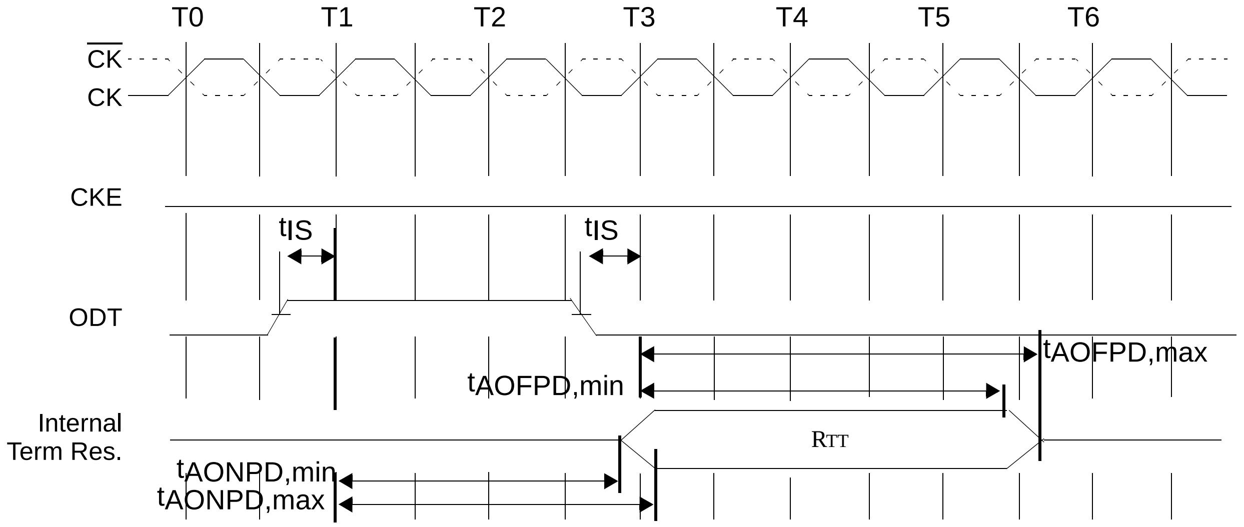


Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

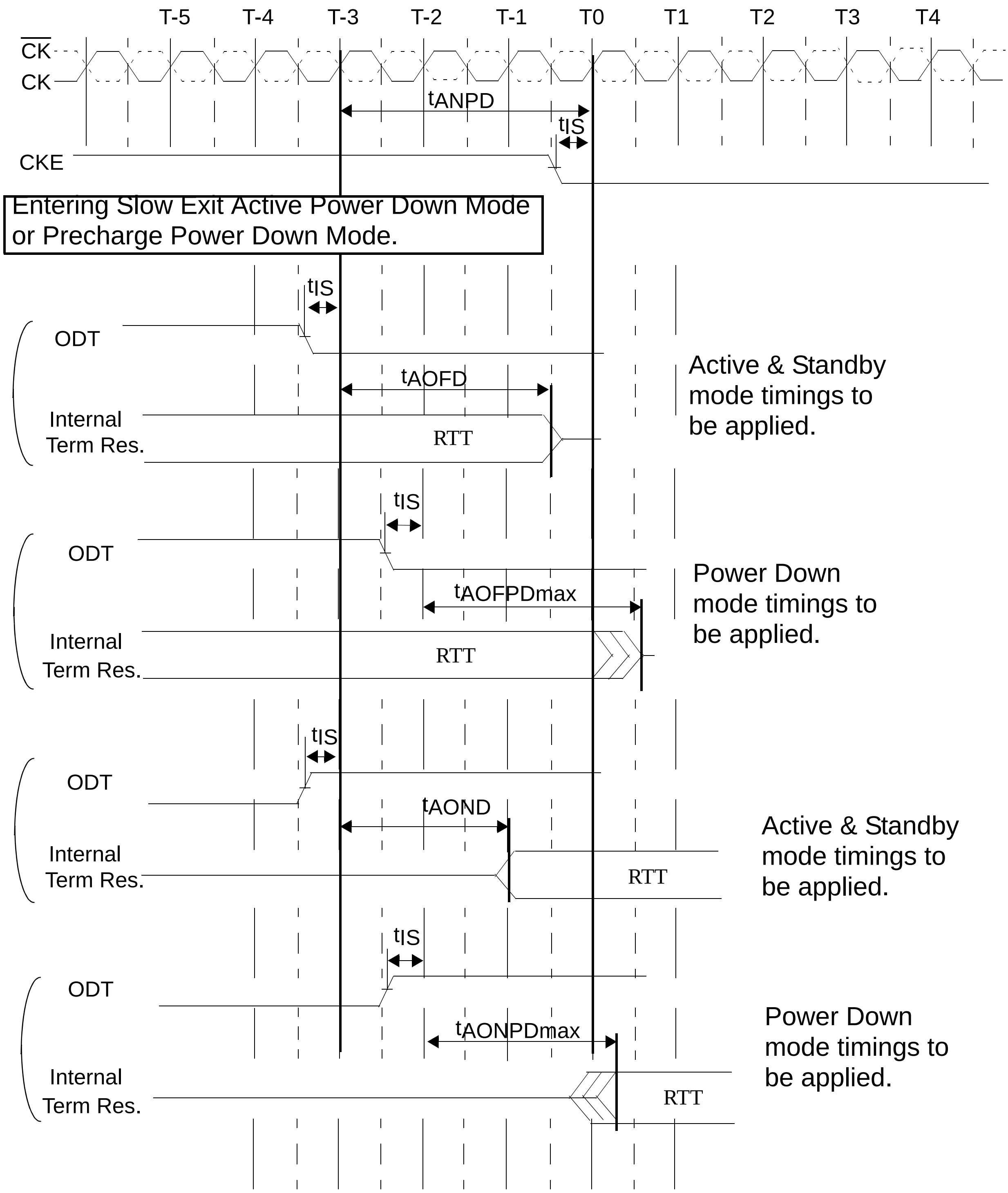
ODT timing for active/standby mode



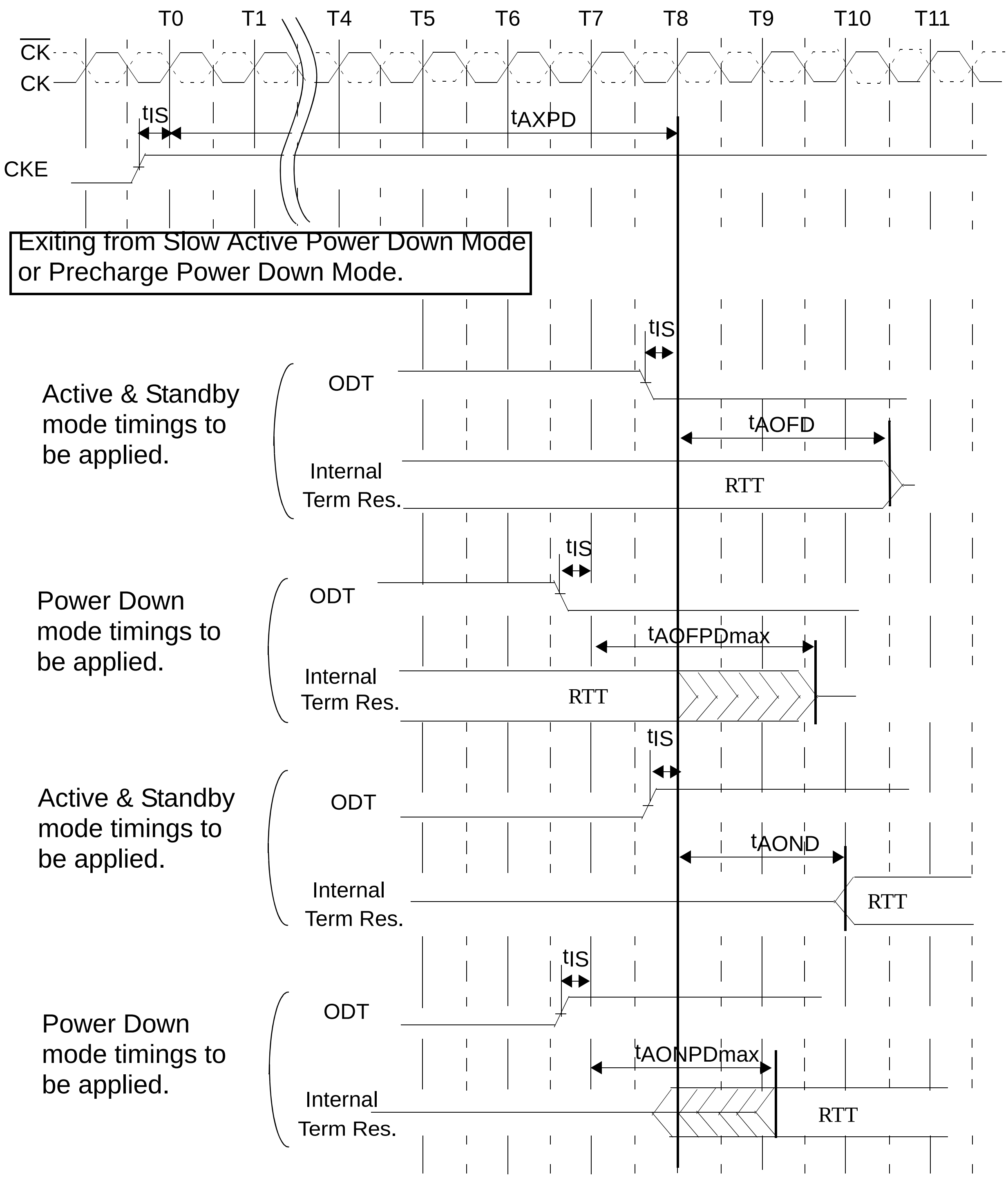
ODT timing for powerdown mode



ODT timing mode switch at entering power down mode



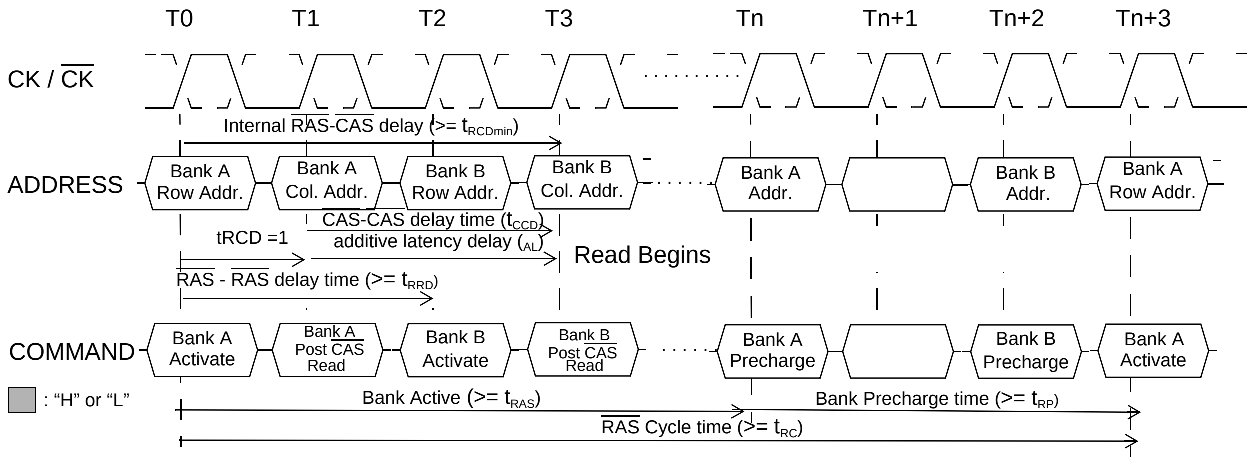
ODT timing mode switch at exiting power down mode



2.4 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4 and 5 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD}.

Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2



2.5 Read and Write Command

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8 bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

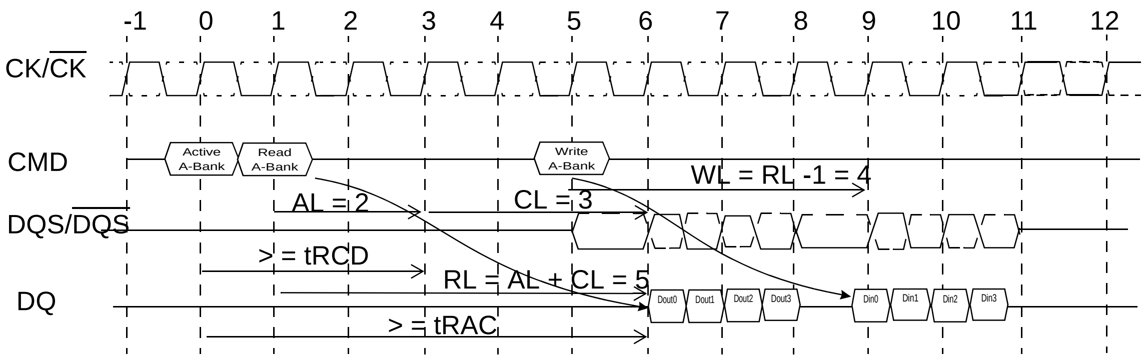
A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundry respectively. The minimum $\overline{CAS}$ to $\overline{CAS}$ delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

2.5.1 Posted CAS

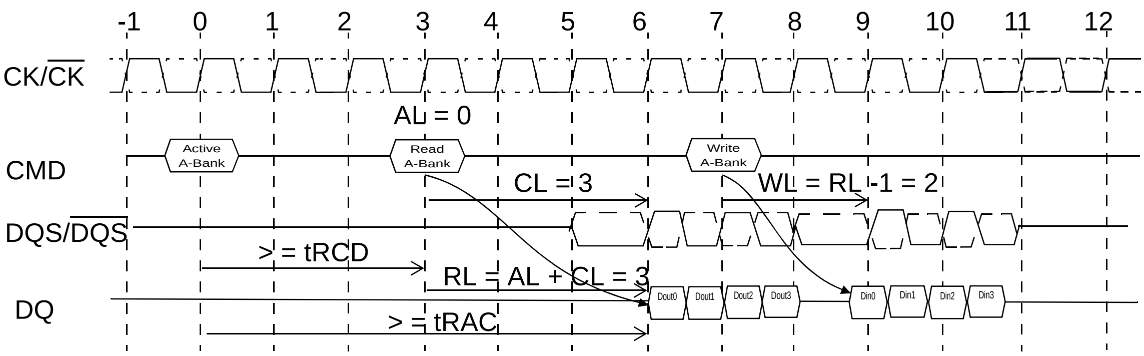
Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a CAS read or write command to be issued immediately after the RAS bank activate command (or any time during the RAS-CAS-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to semaless operation timing diagram examples in Read burst and Wirte burst section)

Examples of posted CAS operation

Example 1 Read followed by a write to the same bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]



Example 2 Read followed by a write to the same bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]



2.5.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: Page length is a function of I/O organization and column addressing

2.5.3 Burst Read Command

The Burst Read command is initiated by having CS and CAS low while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus CAS latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1)(EMRS(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS(1) “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single
ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

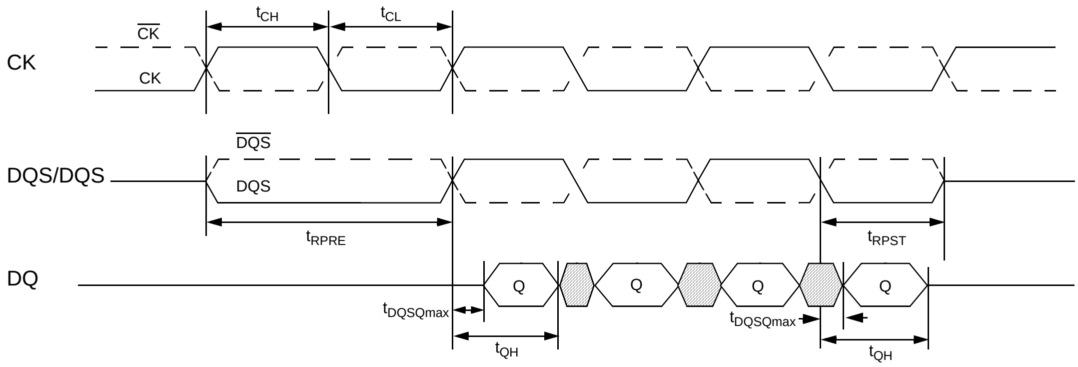
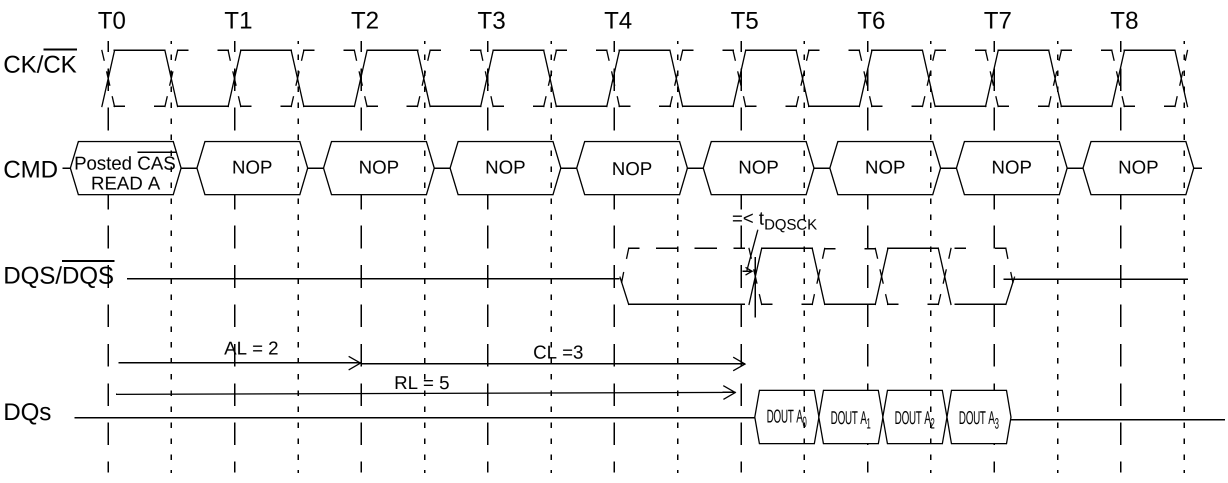
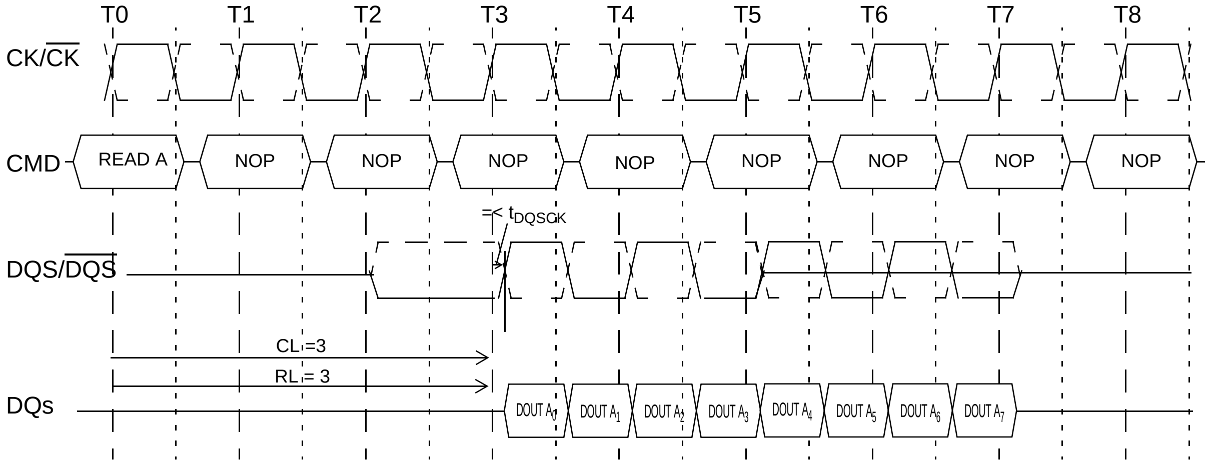


Figure YY-- Data output (read) timing

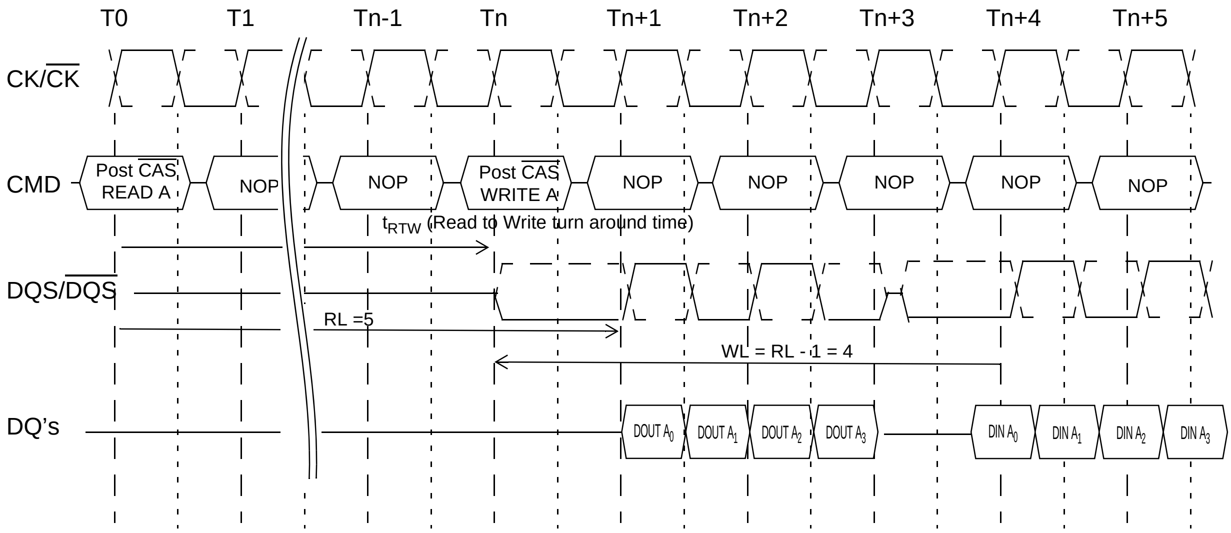
Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

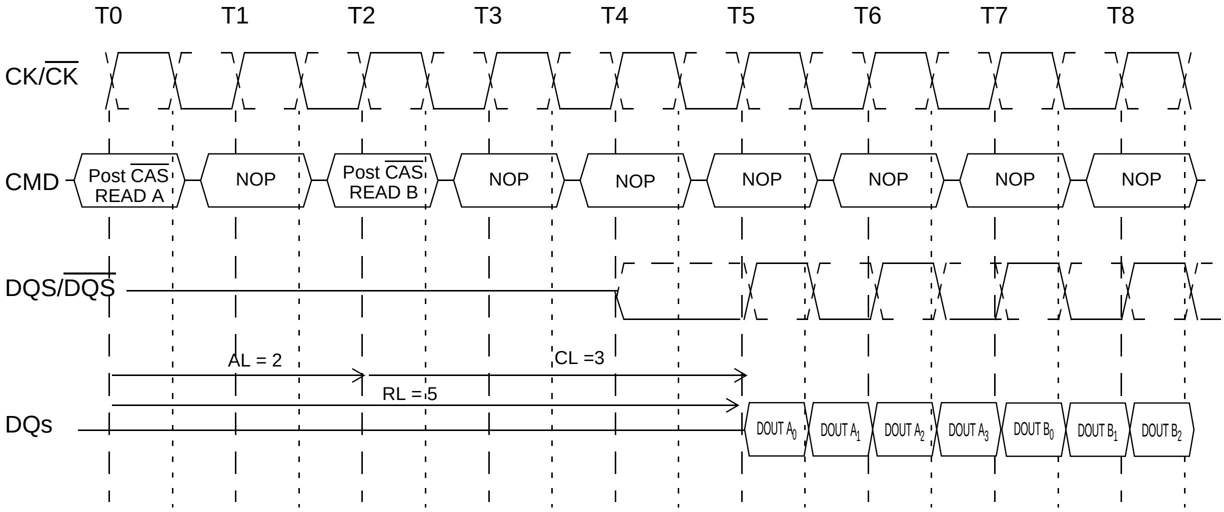


Burst Read followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

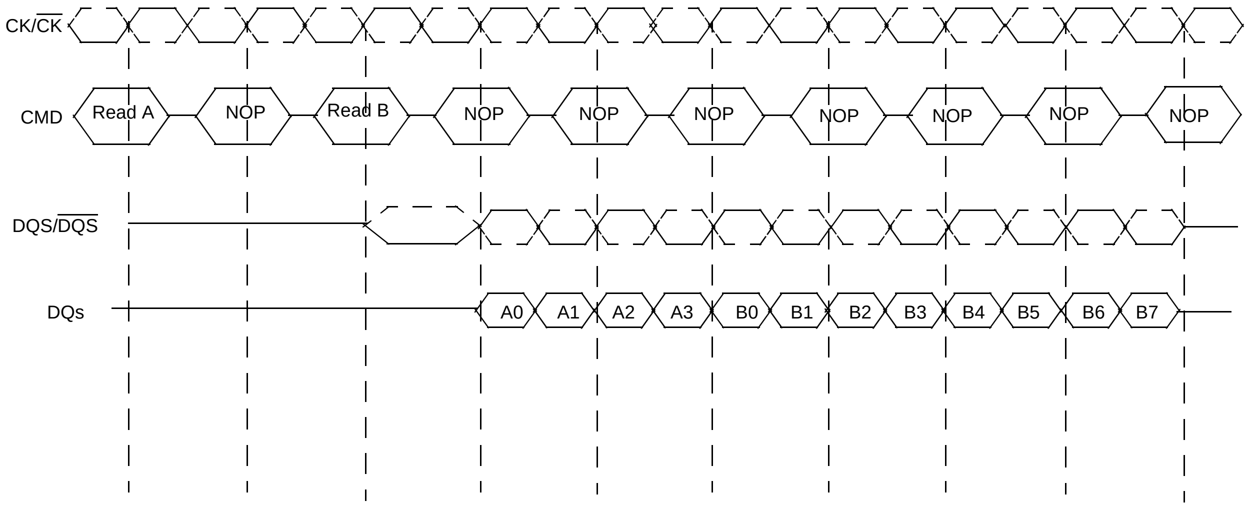


The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Reads interrupted by a read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)

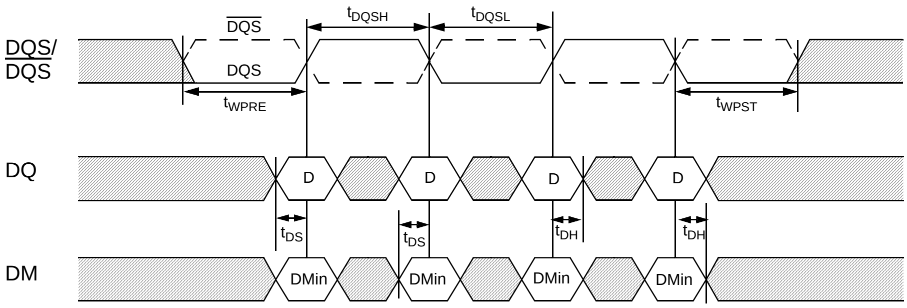


Note

1. Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
3. Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto Precharge enabled is not allowed to interrupt.
6. Read burst interruption is allowed by another Read with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

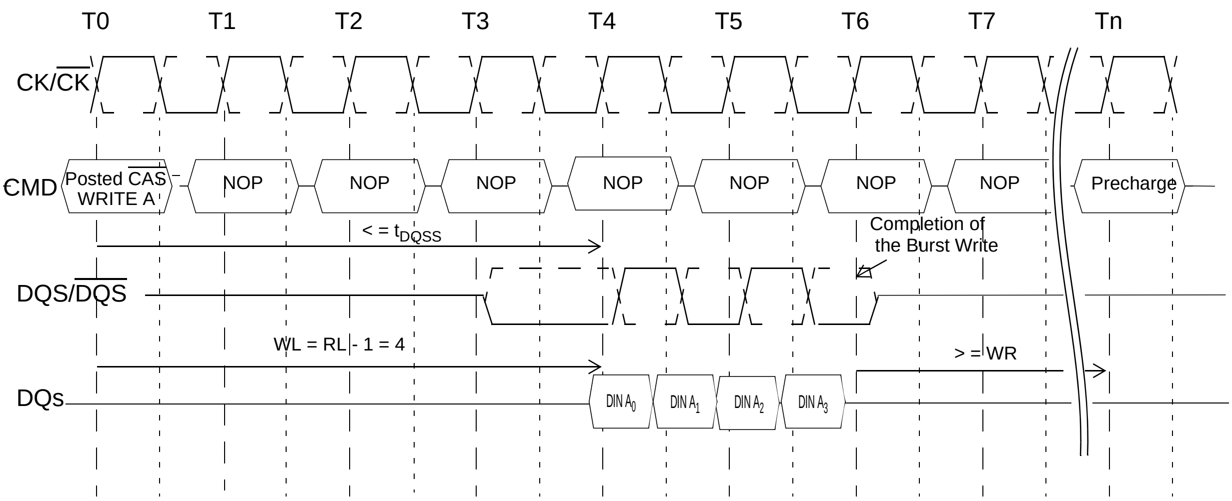
2.5.4 Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).
DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

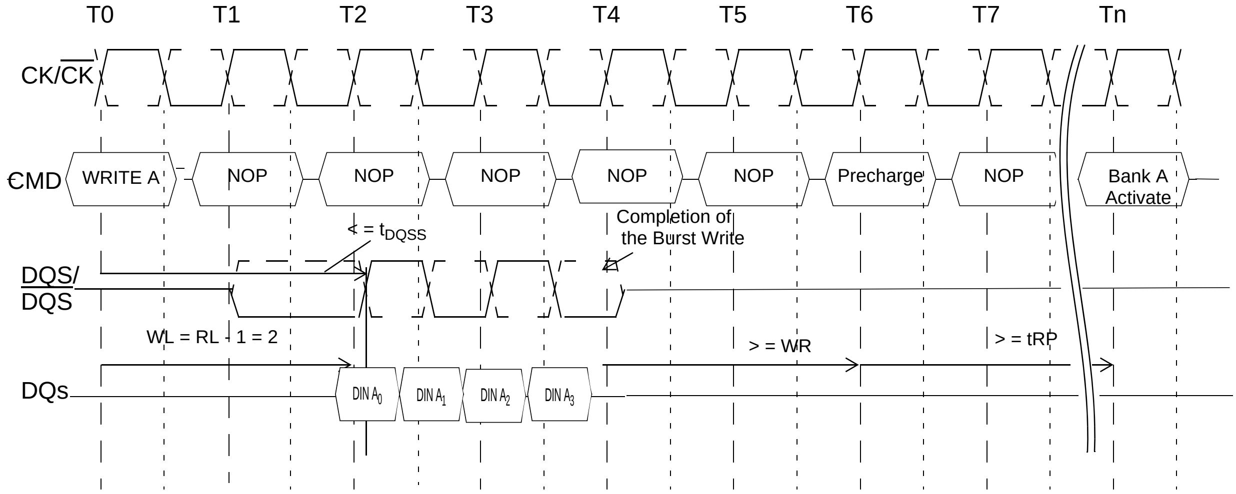


Data input (write) timing

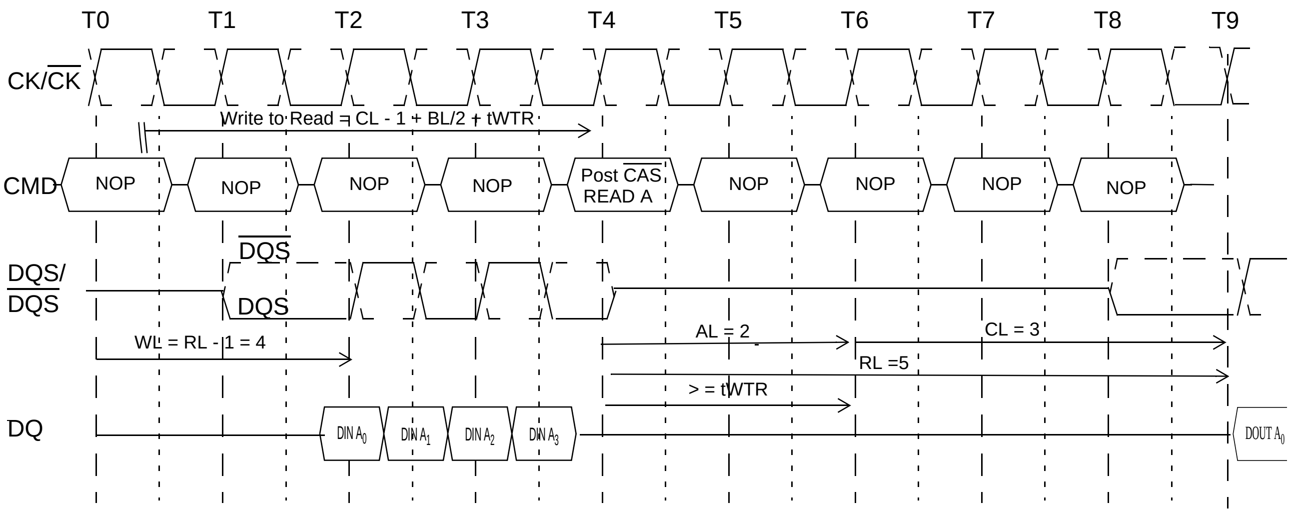
Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL = 4



Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

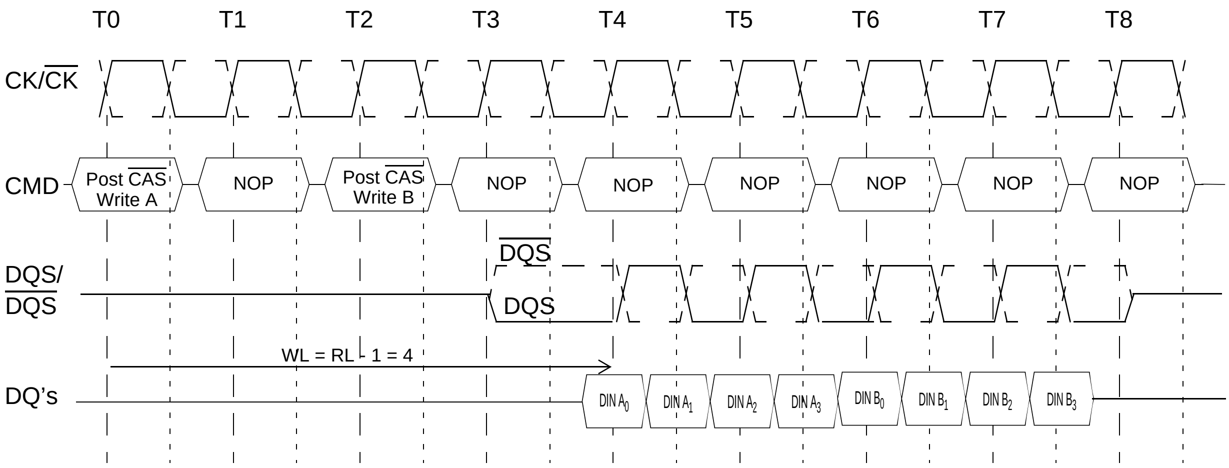


Burst Write followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4



The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

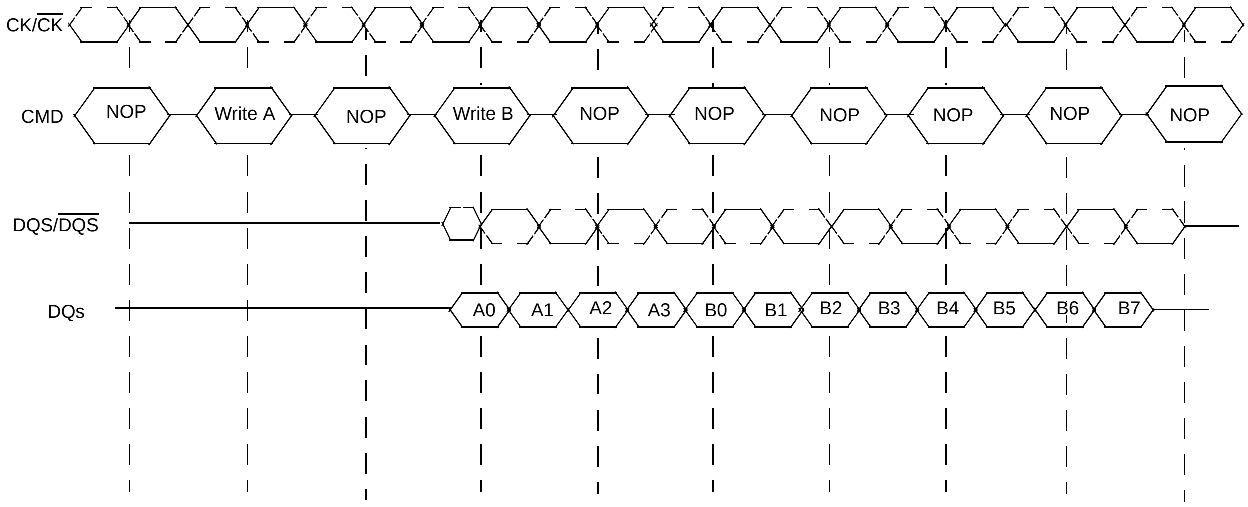


The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated

Writes interrupted by a write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)

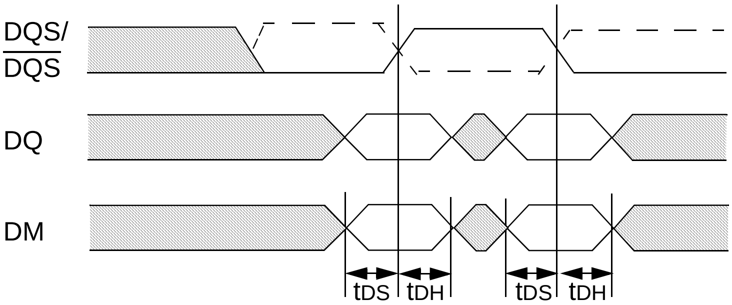


Notes:
1. Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.
3. Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto Precharge enabled is not allowed to interrupt.
6. Write burst interruption is allowed by another Write with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

2.5.5 Write Data Mask

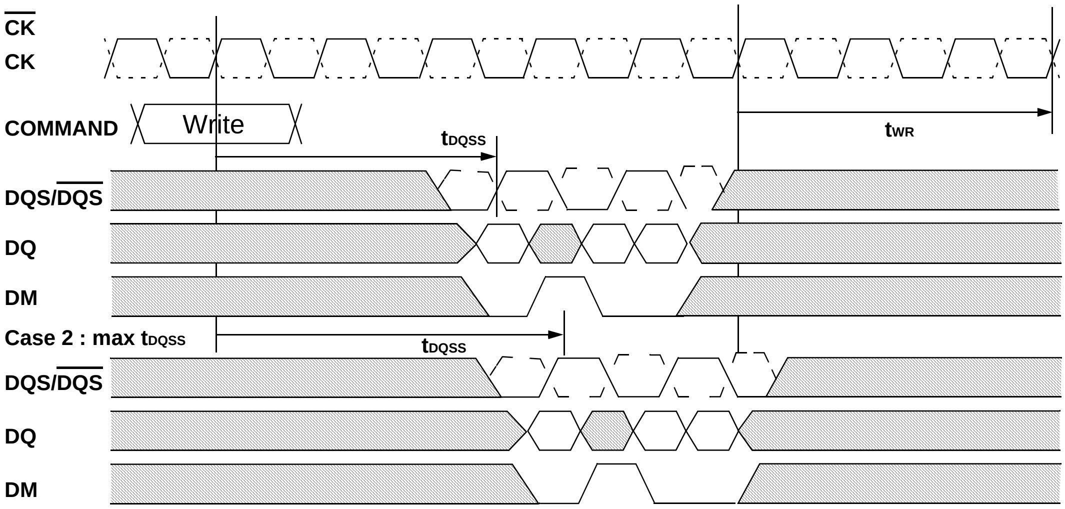
One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, Consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMRS(1) settng.

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1 : min tDQSS



2.6 Precharge Operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 512Mb are used to define which bank to precharge when the command is issued.

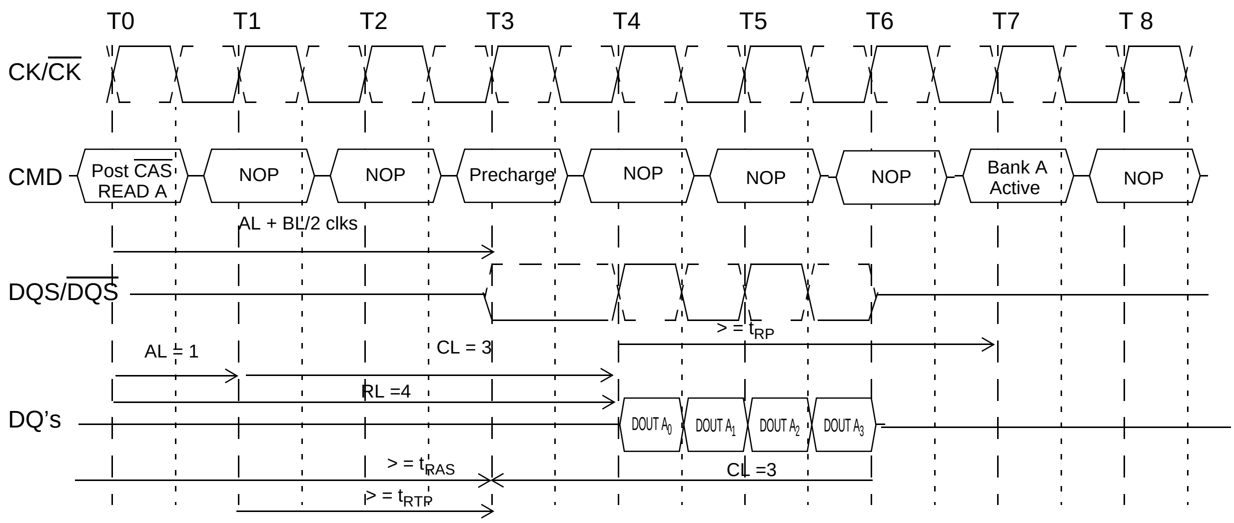
Bank Selection for Precharge by Address Bits

A10	BA1	BA0	Precharged Bank(s)	Remarks
LOW	LOW	LOW	Bank 0 only	
LOW	LOW	HIGH	Bank 1 only	
LOW	HIGH	LOW	Bank 2 only	
LOW	HIGH	HIGH	Bank 3 only	
HIGH	DON'T CARE	DON'T CARE	All Banks	

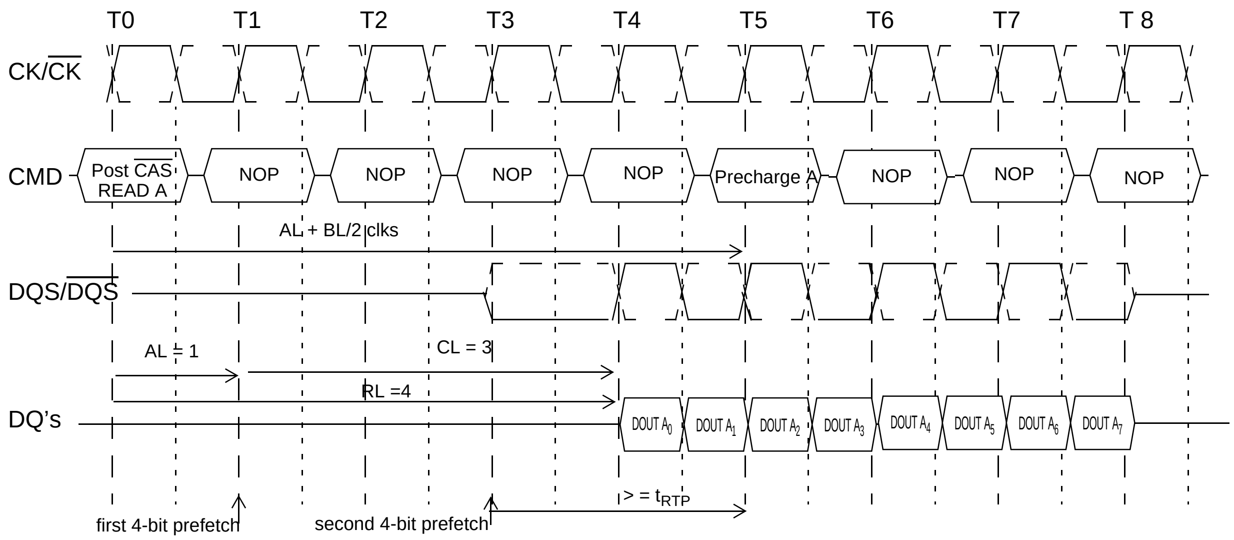
Burst Read Operation Followed by Precharge

Minium Read to precharge command spacing to the same bank = AL + BL/2 clocks
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock egde that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

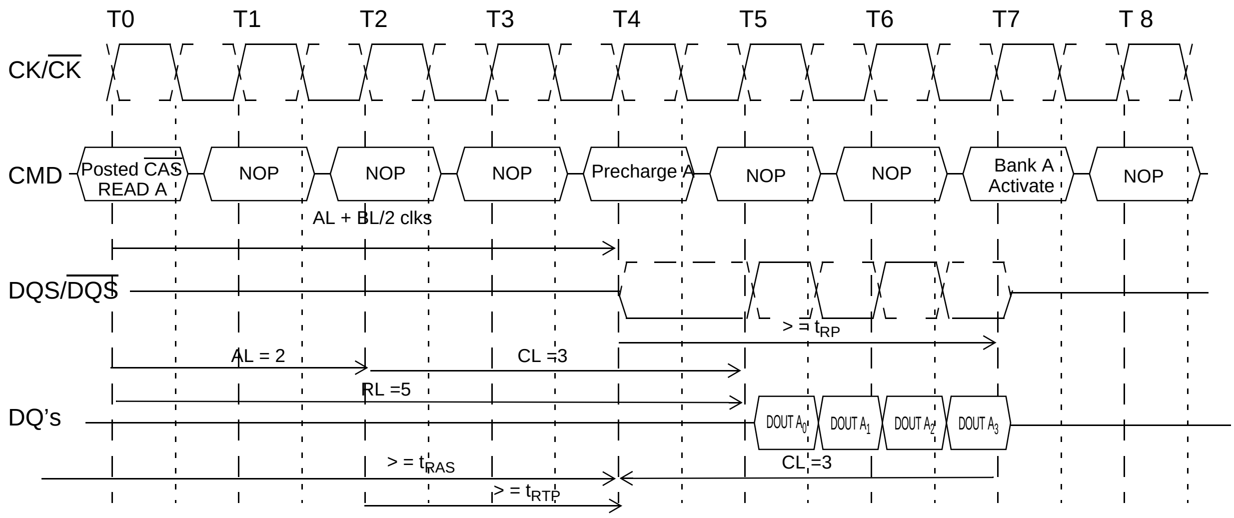
Example 1: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks



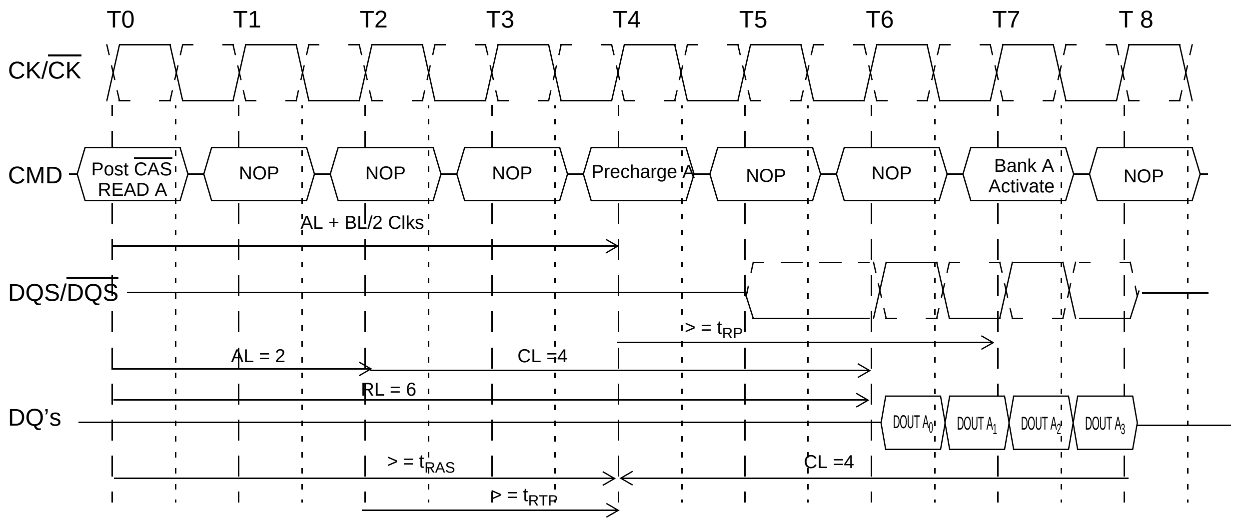
Example 2: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks



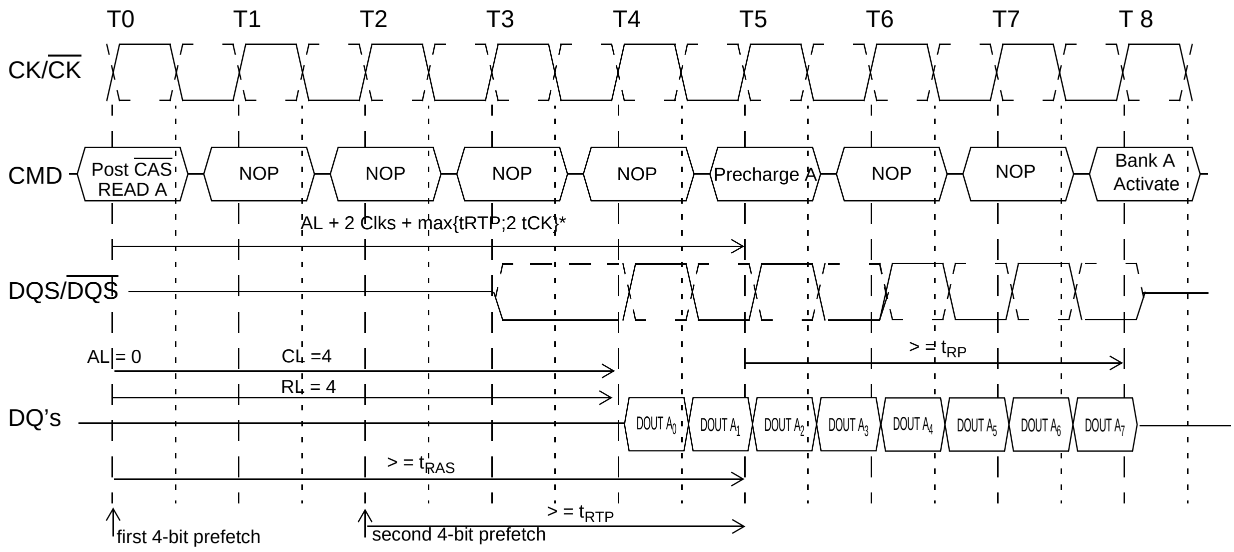
Example 3: Burst Read Operation Followed by Precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks



Example 4: Burst Read Operation Followed by Precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



Example 5: Burst Read Operation Followed by Precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks



* : rounded to next interger