

SERIAL PRESENCE DETECT

Rev. 0.0

Byte	Function described	-D43		-J	
		Function support	HEX	Function support	HEX
0	Number of Bytes written into serial memory at module manufacturer	128 Bytes	80	128 Bytes	80
1	Total Number of Bytes in SPD device	256 Bytes	8	256 Bytes	8
2	Fundmetal Memory Type	DDR SDRAM	07	DDR SDRAM	07
3	Number of Row addresses on this assembly	13	0D	13	0D
4	Number of Column addresses on this assembly	11	0B	11	0B
5	Number of physical banks on DIMM	1	1	1	1
6	Module Data width	64 bit	40	64 bit	40
7	Module data width (continued)	Undefined	0	Undefined	0
8	Module Voltage interface levels (VDDQ)	SSTL2.5	04	SSTL2.5	04
9	DDR SDRAM cycle time at CAS latency =2.5 (tCK)	5.0 ns	50	6.0 ns	60
10	DDR SDRAM Device Access Time from Clock at CL=2.5 (tAC)	+/-0.7ns	70	+/-0.7ns	70
11	Module configuration Type	None	0	None	0
12	Refresh Rate/TYPE	7.8us & Self refresh	82	7.8us & Self refresh	82
13	Primary DDR SDRAM Width	x8	8	x8	8
14	Error Checking DDR SDRAM data width	N/A	0	N/A	0
15	Minimum Clock Delay for back-to-back random column address (tCCD)	1CLK	01	1CLK	01
16	Burst Lengths supported	2,4,8	0E	2,4,8	0E
17	Number of Banks on each DDR SDRAM	4 banks	04	4 banks	04
18	CAS Latency supported	2&2.5&3	1C	2&2.5	0C
19	CS latency	0	01	0	01
20	WE latency	1	02	1	02
21	DDR SDRAM Module Attributes	Differential Clock Input	20	Differential Clock Input	20
22	DDR SDRAM Device Attributes : General	+/-0.2V Tolerance	C0	+/-0.2V Tolerance	C0
23	DDR SDRAM cycle time at CL=2.0 (tCK)	6.0 ns	60	7.5 ns	75
24	DDR SDRAM access time from clock at CL=2.0 (tAC)	+/-0.7ns	70	+/-0.7ns	70
25	DDR SDRAM cycle time at CL=1.5 (tCK),2.0(tCK)	7.5 ns	75		0
26	DDR SDRAM access time from clock at CL=1.5 (tAC)	+/-0.75ns	75		0
27	Minimum row precharge time (tRP)	15 ns	3C	18 ns	48
28	Minimun row active to row active delay (tRRD)	10 ns	28	12 ns	30
29	Minimum RAS to CAS delay (tRCD)	15 ns	3C	18 ns	48
30	Minimum active to precharge time (tRAS)	40 ns	28	42 ns	2A
31	Module row density	512 MBytes	80	512 MBytes	80
32	Command and Address Signal Input Setup Time (tIS)	0.60 ns	60	0.75 ns	75
33	Command and Address Signal Input Hold Time (tIH)	0.60 ns	60	0.75 ns	75
34	Data Signal Input Setup Time (tDS)	0.40 ns	40	0.45 ns	45
35	Date Signal Input Hold Time (tDH)	0.40 ns	40	0.45 ns	45
36-40	Reserved for VCSDRAM	Undefined	00	Undefined	00
41	Minimum active / Auto - Refresh Time (tRC)	55ns	37	60ns	3C
42	Min Auto-Refresh to Active / Auto- Refresh Command period (tRFC)	70 ns	46	72 ns	48
43	Maximum Cycle Time (tCK max)	10ns	28	12ns	30
44	Maximum DQS-DQ skew time (tDQSQ)	0.40 ns	28	0.45 ns	2D
45	Maximum read data hold skew factor (tQHS)	0.50 ns	50	0.55 ns	55
46-61	Superset Information (maybe used in future)	Undefined	00	Undefined	00
62	SPD Revision Code	initial release	00	initial release	00
63	Check SUM for Bytes 0-62		A7		41
64	Manufacturer JEDEC ID Code	Hynix JEDEC ID	AD	Hynix JEDEC ID	AD
65~71	-----Manufacturer JEDEC ID Code		00		00
72	Manufacturing location(See Sheet Name "Byte#72")	Hynix(Korea Area)	0	Hynix(Korea Area)	0
73	Manufacture part number (Hynix Memory Module)	H	48	H	48
74	---Manufacture part number (Hynix Memory Module)	Y	59	Y	59
75	---Manufacture part number (Hynix Memory Module)	M	4D	M	4D
76	Manufacture part number (DDR SDRAM)	D	44	D	44
77	Manufacture part number (Memory Density)	5	35	5	35
78	Manufacture part number (Module depth)	6	36	6	36
79	---Manufacture part number (Module depth)	4	34	4	34
80	Manufacture part number (Module type)	Blank	20	Blank	20
81	Manufacture part number (Data width)	6	36	6	36
82	---Manufacture part number (Data width)	4	34	4	34
83	Manufacture part number (refresh , # of bank)	6	36	6	36
84	Manufacture part number (Component Generation)	C	43	C	43
85	Manufacture part number (Component configuration)	8	38	8	38
86	Manufacture part number (Module Type)/(Hypen)	J	4A	J	4A
87	Manufacture part number (Hypen)/(Minimum cycle time)	-	2D	-	2D
88	Manufacture part number (Miniumum cycle time)	D	44	J	4A
89	Manufacture part number (Miniumum cycle time)	4	34		
90	Manufacture part number (Miniumum cycle time)	3	33	Blank	20
91	Manufacture revision Code (for Component)				
92	Manufacture revision Code (for PCB)				
93	Manufacturing Data (Year)				
94	Manufacturing Data (Week)				
95-98	Module Serial Number(Main Lot NO)-Hexa				
99~127	Manufacturer specific data (may be used in future)	Undefined	00	Undefined	00
128~255	Open for customer use	Undefined	00	Undefined	00

For Lead Free Parts (RoHS Compliant)

Byte	Function described	Function support	HEX	Function support	HEX
85	Manufacture part number (Package Material)	P	50	P	50
86	Manufacture part number (Component configuraion)	8	38	8	38
87	Manufacture part number (Module Type)/(Hypen)	J	4A	J	4A