

## SERIAL PRESENCE DETECT

ID	Function described	HYMP512U64BP8-E3		HYMP512U64BP8-C4		HYMP512U64BP8-Y5		HYMP512U64BP8-S5		HYMP512U64BP8-S6	
		Function support	HEX	Function support	HEX	Function support	HEX	Function support	HEX	Function support	HEX
0	Number of SPD Bytes Written during Module Production	128 Bytes	80	128 Bytes	80	128 Bytes	80	128 Bytes	80	128 Bytes	80
1	Total Number of Bytes in SPD Device	256 Bytes	08	256 Bytes	08	256 Bytes	08	256 Bytes	08	256 Bytes	08
2	Fundamental Memory Type	DDR2 SDRAM	08	DDR2 SDRAM	08	DDR2 SDRAM	08	DDR2 SDRAM	08	DDR2 SDRAM	08
3	Number of Row Addresses on This Assembly	14	0E	14	0E	14	0E	14	0E	14	0E
4	Number of Column Addresses on This Assembly	10	04	10	04	10	04	10	04	10	04
5	Module Height, Package, Number of DIMM Ranks	30.0mm/planar/2rank	61	30.0mm/planar/2rank	61	30.0mm/planar/2rank	61	30.0mm/planar/2rank	61	30.0mm/planar/2rank	61
6	Module Data Width	64	40	64	40	64	40	64	40	64	40
7	Reserved	-	00	-	00	-	00	-	00	-	00
8	Voltage Interface Level of This Assembly	SS1L 1.8V	05	SS1L 1.8V	05	SS1L 1.8V	05	SS1L 1.8V	05	SS1L 1.8V	05
9	SDRAM Cycle Time at CAS Latency =X (tCK)	5.0ns	50	3.75ns	3D	3ns	30	2.5ns	25	2.5ns	25
10	SDRAM Access Time from Clock at CL=X (tAC)	+/-0.6ns	60	+/-0.5ns	50	+/-0.45ns	45	+/-0.40ns	40	+/-0.40ns	40
11	DIMM Configuration Type	No Parity/ECC	00	No Parity/ECC	00	No Parity/ECC	00	No Parity/ECC	00	No Parity/ECC	00
12	Refresh Rate/Type	7.8us	02	7.8us	02	7.8us	02	7.8us	02	7.8us	02
13	Primary SDRAM Width	8	08	8	08	8	08	8	08	8	08
14	Error Checking SDRAM Width	Undefined	00	Undefined	00	Undefined	00	Undefined	00	Undefined	00
15	Reserved	-	00	-	00	-	00	-	00	-	00
16	Burst Lengths Supported	4,8	0C	4,8	0C	4,8	0C	4,8	0C	4,8	0C
17	Number of Banks on Each SDRAM Device	4	04	4	04	4	04	4	04	4	04
18	CAS Latency	3,4,5	38	3,4,5	38	3,4,5	38	3,4,5	38	4,5,6	70
19	DIMM Mechanical characteristics; thickness	≤ 4.10mm	01	≤ 4.10mm	01	≤ 4.10mm	01	≤ 4.10mm	01	≤ 4.10mm	01
20	DIMM Type	Regular UDIMM	02	Regular UDIMM	02	Regular UDIMM	02	Regular UDIMM	02	Regular UDIMM	02
21	SDRAM Device Attributes : General	Undefined	00	Undefined	00	Undefined	00	Undefined	00	Undefined	00
22	SDRAM Device Attributes : General	PASR/ODT 50Q/Weak Driver	07	PASR/ODT 50Q/Weak Driver	07	PASR/ODT 50Q/Weak Driver	07	PASR/ODT 50Q/Weak Driver	07	PASR/ODT 50Q/Weak Driver	07
23	SDRAM Cycle Time at CL=X-1 (tCK)	5.0ns	50	3.75ns	3D	3.75ns	3D	3.75ns	3D	3ns	30
24	SDRAM Access Time from Clock at CL=X-1 (tAC)	+/-0.6ns	60	+/-0.5ns	50	+/-0.5ns	50	+/-0.5ns	50	+/-0.45ns	45
25	SDRAM Cycle Time at CL=X-2 (tCK)	5.0ns	50	5.0ns	50	5.0ns	50	5.0ns	50	3.75ns	3D
26	SDRAM Access Time from Clock at CL=X-2 (tAC)	+/-0.6ns	60	+/-0.6ns	60	+/-0.6ns	60	+/-0.6ns	60	+/-0.5ns	50
27	Minimum Row Precharge Time (tRP)	15ns	3C	15ns	3C	15ns	3C	12.5ns	32	15ns	3C
28	Minimum Row Active to Row Active Delay (tRRD)	7.5ns	1E	7.5ns	1E	7.5ns	1E	7.5ns	1E	7.5ns	1E
29	Minimum RAS to CAS Delay (tRCD)	15ns	3C	15ns	3C	15ns	3C	12.5ns	32	15ns	3C
30	Minimum Active to Precharge Time (tRAS)	40ns	28	45ns	2D	45ns	2D	45ns	2D	45ns	2D
31	Module Rank Density	512MB	80	512MB	80	512MB	80	512MB	80	512MB	80
32	Command and Address Signal Input Setup Time (tIS)	0.25ns	35	0.25ns	25	0.20ns	20	0.175ns	17	0.175ns	17
33	Command and Address Signal Input Hold Time (tIH)	0.475ns	47	0.375ns	37	0.275ns	27	0.250ns	25	0.250ns	25
34	Data Signal Input Setup Time (tDS)	0.15ns	15	0.1ns	10	0.10ns	10	0.050 ns	05	0.050 ns	05
35	Data Signal Input Hold Time (tDH)	0.275ns	27	0.225ns	22	0.175ns	17	0.125ns	12	0.125ns	12
36	Write Recovery Time (tWR)	15ns	3C	15ns	3C	15ns	3C	15ns	3C	15ns	3C
37	Internal Write to Read Command Delay (tWTR)	10ns	28	7.5ns	1E	7.5ns	1E	7.5ns	1E	7.5ns	1E
38	Internal Read to Precharge Command Delay (tRTP)	7.5ns	1E	7.5ns	1E	7.5ns	1E	7.5ns	1E	7.5ns	1E
39	Memory Analysis Probe Characteristics	N/A	00	N/A	00	N/A	00	N/A	00	N/A	00
40	Extension of Byte 41 tRFC and Byte 42 tRFC	No extension needed	00	No extension needed	00	No extension needed	00	Extension of byte41	30	No extension needed	00
41	Minimum Active to Active / Auto - Refresh Time ( tRC)	55ns	37	60ns	3C	60ns	3C	57.5ns	39	60ns	3C
42	Min Auto-Refresh to Active / Auto- Refresh Command period (tRFC)	105ns	69	105ns	69	105ns	69	105ns	69	105ns	69
43	Maximum Cycle Time ( tCK max)	8.0ns	80	8.0ns	80	8.0ns	80	8.0ns	80	8.0ns	80
44	Maximum DQS-DQ skew time (tDQSQ)	0.35ns	23	0.3ns	1E	0.24ns	18	0.200ns	14	0.200ns	14
45	Maximum Read Data Hold Skew Factor (tQHS)	0.45ns	2D	0.4ns	28	0.34ns	22	0.300ns	1E	0.300ns	1E
46	PLL Relock Time	No PLL	00	No PLL	00	No PLL	00	No PLL	00	No PLL	00
47	DRAM Tcase max/DT4RW mode bit	95 C / 1.3 C	53	95 C / 2.6 C	37	95 C / 1.3 C	53	Undefined	00	Undefined	00
48	Thermal resistance of DRAM Package from Top(Case) to Ambient.	69 C/W	84	69 C/W	84	69 C/W	84	Undefined	00	Undefined	00
49	DRAM Tcase Rise in IDD0 condition/Mode Bits(DT0/Mode Bits)	7.7 C support / support	6B	7.7 C support / support	6B	9 C support / support	7B	Undefined	00	Undefined	00
50	DRAM Tcase Rise in IDD2N or IDD2O condition(DT2N/DT2O)	4.6 C	2E	5.9 C	3B	6.6 C	42	Undefined	00	Undefined	00

51	DRAM Tcse Rise in IDD2P condition(DT2P)	1 C	46	1 C	46	1 C	46	Undefined	00	Undefined	00
52	DRAM Tcse Rise in IDD3N condition(DT3N)	6.6 C	2C	7.2 C	30	7.9 C	34	Undefined	00	Undefined	00
53	DRAM Tcse Rise in IDD3P-fast condition(DT3Pfast)	3.9 C	4F	3.9 C	4F	4.6 C	5C	Undefined	00	Undefined	00
54	DRAM Tcse Rise in IDD3P-slow condition(DT3P slow)	1.6 C	3F	1.6 C	3F	1.6 C	3F	Undefined	00	Undefined	00
55	DRAM Tcse Rise in IDD4RW condition/Mode Bit(DT4R)	17 C / IDD4W greater	56	19.7 C / IDD4W greater	62	23.6 C / IDD4W greater	76	Undefined	00	Undefined	00
56	DRAM Tcse Rise in IDD5B condition(DT5B)	21 C	2A	22.1 C	2D	23.6 C	2F	Undefined	00	Undefined	00
57	DRAM Tcse Rise in IDD7 condition(DT7)	28.8 C	3A	28.8 C	3A	28.8 C	3A	Undefined	00	Undefined	00
58-61	SPD Bytes for R-DIMM	N/A	00	N/A	00	N/A	00	N/A	00	N/A	00
62	SPD Revision Code	1.2	12	1.2	12	1.2	12	1.2	12	1.2	12
63	Check SUM for Bytes 0-62	-	E4	-	8E	-	84	-	9C	-	00
64	Manufacturer JEDEC ID Code	Hynix JEDEC ID	AD	Hynix JEDEC ID	AD	Hynix JEDEC ID	AD	Hynix JEDEC ID	AD	Hynix JEDEC ID	AD
65-71	-----Manufacturer JEDEC ID Code	-	00	-	00	-	00	-	00	-	00
72	Manufacturing location(See Sheet Name "Byte#72")	Hynix(fchon)	01	Hynix(fchon)	01	Hynix(fchon)	01	Hynix(fchon)	01	Hynix(fchon)	01
73	Manufacture part number ( Hynix Memory Module )	H	48	H	48	H	48	H	48	H	48
74	-----Manufacture part number ( Hynix Memory Module )	Y	59	Y	59	Y	59	Y	59	Y	59
75	-----Manufacture part number ( Hynix Memory Module )	M	4D	M	4D	M	4D	M	4D	M	4D
76	Component group (DDR2 SDRAM)	P	50	P	50	P	50	P	50	P	50
77	-----Component group(DDR2 SDRAM)	5	35	5	35	5	35	5	35	5	35
78	Manufacture part number ( Module depth )	1	31	1	31	1	31	1	31	1	31
79	-----Manufacture part number ( Module depth )	2	32	2	32	2	32	2	32	2	32
80	Manufacture part number ( Module type )	U	55	U	55	U	55	U	55	U	55
81	Manufacture part number ( Data width )	6	36	6	36	6	36	6	36	6	36
82	-----Manufacture part number ( Data width )	4	34	4	34	4	34	4	34	4	34
83	Manufacture part number ( Component generation)	B	42	B	42	B	42	B	42	B	42
84	Manufacture part number ( Package Materials)	P	50	P	50	P	50	P	50	P	50
85	Manufacture part number ( Component configuration)	8	38	8	38	8	38	8	38	8	38
86	Manufacture part number ( Hyphen )	-	2D	-	2D	-	2D	-	2D	-	2D
87	Manufacture part number ( Minimum cycle time )	E	43	C	43	Y	59	S	53	S	53
88	-----Manufacture part number ( Minimum cycle time )	3	33	4	34	5	35	5	35	6	36
89-90	Manufacture part number ( T.B.D)	Blank	20	Blank	20	Blank	20	Blank	20	Blank	20
91	Manufacture revision Code ( for Component )										
92	Manufacture revision Code ( for PCB )										
93	Manufacturing Data ( Year )										
94	Manufacturing Data ( Week )										
95-98	Module Serial Number(Main Lot NO)-Hexa										
99-127	Manufacturer specific data ( may be used in future)	Undefined	00	Undefined	00	Undefined	00	Undefined	00	Undefined	00
128-255	Open for customer use	Undefined	00	Undefined	00	Undefined	00	Undefined	00	Undefined	00

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