SERIAL PRESENCE DETECT

		E3		C4	
	Function described	Function support	HEX	Function support	HEX
0	Number of SPD Bytes Written during Module Production	128 Bytes	80	128 Bytes	80
1	Total Number of Bytes in SPD Device	256 Bytes	08	256 Bytes	08
2	Fundmetal Memory Type	DDR2 SDRAM	08	DDR2 SDRAM	08
3	Number of Row Addresses on This Assembly	14	0E	14	0E
4	Number of Column Addresses on This Assembly	10	0A	10	0A
5	Module Height, Package, Number of DIMM Ranks	30.0mm/ planar/ 2rank	61	30.0mm/ planar/ 2rank	61
6	Module Data Width	64	40	64	40
7	Reserved	-	00	-	00
8	Voltage Interface Level of This Assembly	SSTL 1.8V	05	SSTL 1.8V	05
9	SDRAM Cycle Time at CAS Latency =4 (tCK)	5.0ns	50	3.75ns	3D
10	SDRAM Access Time from Clock at CL=4 (tAC)	+/-0.6ns	60	+/-0.5ns	50
11	DIMM Configuration Type	No Parity/ECC	00	No Parity/ECC	00
12	Refresh Rate/Type	7.8us	02	7.8us	02
13	Primary SDRAM Width	8	08	8	08
14	Error Checking SDRAM Width	Undefined	00	Undefined	00
15	Reserved	-	00	-	00
16	Burst Lengths Suppoted	4,8	0C	4,8	0C
17	Number of Banks on Each SDRAM Device	4	04	4	04
18	CAS Latency	3,4,5	38	3,4,5	38
19	DIMM Mechanical characteristics; thickness	≤ 4.10mm	01	≤ 4.10mm	01
20	DIMM Type	Regular UDIMM	02	Regular UDIMM	02
21	SDRAM Device Attributes : General	Undefined	00	Undefined	00
22	SDRAM Device Attributes : General	Supports Weak Driver	01	Supports Weak Driver	01
23	SDRAM Cycle Time at CL=4 (tCk)	5.0ns	50	3.75ns	3D
24	SDRAM Access Time from Clock at CL=4 (tAC)	+/-0.6ns	60	+/-0.5ns	50
25	SDRAM Cycle Time at CL=3 (tCk)	5.0ns	50	5.0ns	50
26	SDRAM Access Time from Clock at CL=3 (tAC)	+/-0.6ns	60	+/-0.6ns	60
27	Minimum Row Precharge Time (tRP)	15ns	3C	15ns	3C
28	Minimun Row Active to Row Active Delay (tRRD)	7.5ns	1E	7.5ns	1E
29	Minimum RAS to CAS Delay (tRCD)	15ns	3C	15ns	3C
30	Minimum Active to Precharge Time (tRAS)	40ns	28	45ns	2D
31	Module Rank Density	512MB	80	512MB	80
32	Command and Address Signal Input Setup Time (tIS)	0.35ns	35	0.25ns	25
33	Command and Address Signal Input Hold Time (tIH)	0.475ns	47	0.375ns	37
34	Data Signal Input Setup Time (tDS)	0.15ns	15	0.1ns	10
35	Date Signal Input Hold Time (tDH)	0.275ns	27	0.225ns	22
36	Write Recovery Time (tWR)	15ns	3C	15ns	3C
37	Internal Write to Read Command Delay (tWTR)	10ns	28	7.5ns	1E
38	Internal Read to Precharge Command Delay (tRTP)	7.5ns	1E	7.5ns	1E
39	Memory Analysis Probe Characteristics	N/A	00	N/A	00
40	Extension of Byte 41 tRC and Byte 42 tRFC	No extension needed	00	No extension needed	00
41	Minimum Active to Active / Auto - Refresh Time (tRC)	55ns	37	60ns	3C
42	Min Auto-Refresh to Active / Auto- Refresh Command period (tRFC)	105ns	69	105ns	69
43	Maximum Cycle Time (tCK max)	8.0ns	80	8.0ns	80
44	Maximum DQS-DQ skew time (tDQSQ)	0.35ns	23	0.3ns	1E
45	Maximum Read Data Hold Skew Factor (tQHS)	0.45ns	2D	0.4ns	28
46	PLL Relock Time	No PLL	00	No PLL	00
47	DRAM Tcase max/DT4R4W mode bit	95℃/ 2.4℃	56	95℃/ 2.4℃	56
48	Thermal resistance of DRAM Package from Top(Case) to Ambient.	59℃/W	76	59℃/W	76
49	DRAM Tcase Rise in IDD0 condtion/Mode Bits(DT0/Mode Bits)	6.3℃/ High temp. support	57	7.2℃/ High temp. support	63
50	DRAM Tcase Rise in IDD2N or IDD2Q condition(DT2N/DT2Q)	4.5℃	2D	5℃	32
51	DRAM Tcase Rise in IDD2P condition(DT2P)	0.555℃	25	0.675℃	2D
52	DRAM Tcase Rise in IDD3N condition(DT3N)	6.15℃	29	7.35℃	31
53	DRAM Tcase Rise in IDD3P-fast condition(DT3Pfast)	2.25℃	2D	2.8℃	38
54	DRAM Tcase Rise in IDD3P-slow condition(DT3P slow)	0.55℃	16	0.675℃	1B
55	DRAM Tcase Rise in IDD4RW condition/Mode Bit(DT4R)	14.4℃/ DT4W greater	48	18℃/ DT4W greater	5A
56	DRAM Tcase Rise in IDD5B condtion(DT5B)	18.5℃	25	19.5℃	27
57	DRAM Tcase Rise in IDD7 condtion(DT7)	24.5℃	31	24.5℃	31
58~61	SPD Bytes for R-DIMM	N/A	00	N/A	00
62	SPD Revision Code	1.2	12	1.2	12
63	Check SUM for Bytes 0-62	-	2D	-	F8

SERIAL PRESENCE DETECT

		E3		C4	
	Function described	Function support	HEX	Function support	HEX
64	Manufacturer JEDEC ID Code	**Hynix JEDEC ID**	AD	**Hynix JEDEC ID**	AD
65~71	----------Manufacturer JEDEC ID Code	-	00	-	00
72	Manufacturing location(See Sheet Name "Byte#72")	Hynix(Ichon)	01	Hynix(Ichon)	01
73	Manufacture part number (Hynix Memory Module)	H	48	H	48
74	~~~~Manufacture part number (Hynix Memory Module)	Y	59	Y	59
75	~~~~Manufacture part number (Hynix Memory Module)	M	4D	M	4D
76	Component group (DDR2 SDRAM)	P	50	P	50
77	~~~Component group(DDR2 SDRAM)	5	35	5	35
78	Manufacture part number (Module depth)	1	31	1	31
79	~~~~Manufacture part number (Module depth)	2	32	2	32
80	Manufacture part number (Module type)	U	55	U	55
81	Manufacture part number (Data width)	6	36	6	36
82	~~~~Manufacture part number (Data width)	4	34	4	34
83	Manufacture part number (Package Material)	P	50	P	50
84	Manufacture part number (Component configuration)	8	38	8	38
85	Manufacture part number (Hyphen)	-	2D	-	2D
86	Manufacture part number (Minimum cycle time)	E	45	C	43
87	~~~Manufacture part number (Minimum cycle time)	3	33	4	34
88~90	Manufacture part number (T.B.D)	Blank	20	Blank	20
91	Manufacture revision Code (for Componuent)				
92	Manufacture revision Code (for PCB)				
93	Manufacturing Data (Year)				
94	Manufacturing Data (Week)				
95-98	Module Serial Number(Main Lot N0)-Hexa				
99~127	Manufacturer specific data (may be used in future)	Undefined	00	Undefined	00
128~255	Open for customer use	Undefined	00	Undefined	00

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