



SERIAL PRESENCE DETECT

SERIAL PRESENCE DETECT		HYMP564F72CP8N3-C4		HYMP564F72CP8N3-Y5	
	Function described	Function support	HEX	Function support	HEX
0	Number of Serial PD Bytes written/SPD Device Size/CRC Coverage	176 /256 / 116 Bytes	92	176 /256 / 116 Bytes	92
1	SPD Revision	1.1	11	1.1	11
2	Key Byte / DRAM Device Type	DDR2 SDRAM FB-DIMM	09	DDR2 SDRAM FB-DIMM	09
3	Voltage Levels of this Assembly	1.5V / 1.8V	12	1.5V / 1.8V	12
4	SDRAM Addressing(Row /Column / Bank)	14 / 10 / 4	44	14 / 10 / 4	44
5	Module Physical Attributes	30.35mm/ 8mm	23	30.35mm/ 8mm	23
6	Module Type / Thickness	FB-DIMM	07	FB-DIMM	07
7	Module Organization	1R/ x8	09	1R/ x8	09
8	Fine Timebase Dividened	10 ps / 1	A1	10 ps / 1	A1
9	Medium Timebase Dividened and Divisor	1ns	01	1ns	01
10	Medium Timebase Divisor	4	04	4	04
11	SDRAM Minimum Cycle Time(tCKmin)	3.75ns	0F	3ns	0C
12	SDRAM Maximum Cycle Time(tCKmax)	8ns	20	8ns	20
13	SDRAM CAS Latency Supported	3,4	23	4,5	24
14	SDRAM Minimum CAS Latency Time(tAA)	DDR2 533 4-4-4	3C	DDR2 667 5-5-5	3C
15	SDRAM Write Recovery Times Supported	2,3,4	32	2,3,4,5	42
16	SDRAM Write Recovery Time(tWR)	15ns	3C	15ns	3C
17	SDRAM Write Latency Supported	2,3,4,5	42	2,3,4,5	42
18	SDRAM Additive Latency Supported	0,1,2,3	40	0,1,2,3	40
19	SDRAM Minimum RAS to CAS Delay (tRCD)	15ns	3C	15ns	3C
20	SDRAM Minimum Row Active to Row Active Delay (tRRD)	7.5ns	1E	7.5ns	1E
21	SDRAM Minimum Row Precharge Time (tRP)	15ns	3C	15ns	3C
22	SDRAM Upper Nibbles for tRAS and tRC	Undefined	00	Undefined	00
23	SDRAM Minimum Active to Precharge Time (tRAS)	45ns	B4	45ns	B4
24	SDRAM Minimum Active to Active / Auto - Refresh Time (tRC)	60ns	F0	60ns	F0
25	SDRAM Min Auto-Refresh to Active / Auto- Refresh Command period (tRFC)	105ns	A4	105ns	A4
26	SDRAM Min Auto-Refresh to Active / Auto- Refresh Command period (tRFC)	105ns	01	105ns	01
27	SDRAM Internal Write to Read Command Delay (tWTR)	7.5ns	1E	7.5ns	1E
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	7.5ns	1E	7.5ns	1E
29	SDRAM Burst Lengths Supported	4,8	03	4,8	03
30	SDRAM Termination Supported	50/ 75/ 150Ω	07	50/ 75/ 150Ω	07
31	SDRAM Drivers Supported	Weak driver	01	Weak driver	01
32	SDRAM Average Refresh Interval(tREFI)/Double Refresh mode bit/ High Temperature self-refresh rate support indication	7.8us/ Double Ref./High temp. self ref.	C2	7.8us/ Double Ref./High temp. self ref.	C2
33	DRAM Tcase max / DT4R4W mode bit		57		57
34	Thermal resistance of DRAM Package from Top(Case) to Ambient.		90		90
35	DRAM Tcase Rise in IDD0 condition/Mode Bits(DT0)		6C		80
36	DRAM Tcase Rise in IDD2Q condition(DT2Q)		29		37
37	DRAM Tcase Rise in IDD2P condition(DT2P)		24		24
38	DRAM Tcase Rise in IDD3N condition(DT3N)		2E		2E
39	DRAM Tcase Rise in IDD4RW condition/Mode Bit(DT4R)		44		52
40	DRAM Tcase Rise in IDD5B condition(DT5B)		29		2C
41	DRAM Tcase Rise in IDD7 condition(DT7)		39		3C
42-78	Reserved	Undefined	00	Undefined	00
79	FB-DIMM ODT values		01		01
80	Reserved	Undefined	00	Undefined	00
81	FBD Channel Protocols Supported	ECC	02	ECC	02
82	FBD Channel Protocols Supported	Undefined	00	Undefined	00
83	Back-to-Back Access Turnaround Time		10		10
84	AMB Read Access Delay for AMB.LINKPARNXT[1:0]=11		56		56
85	AMB Read Access Delay for AMB.LINKPARNXT[1:0]=10		40		40
86	AMB Read Access Delay for AMB.LINKPARNXT[1:0]=01		36		36
87	Thermal Resistance of AMB Package(Psi T-A DRAM)		30		30
88	AMB DT idle_0		52		60
89	AMB DT idle_1		66		7A
90	AMB DT idle_2		60		6E

91	AMB DT Active_1		84		A1
92	AMB DT Active_2		6A		7F
93	AMB DT L0s	Undefined	00	Undefined	00
94-97	Reserved	Undefined	00	Undefined	00
98	AMB Tjmax	110℃	00	110℃	00
99	Airflow impedance and category bits		8A		8A
100	Reserved	Undefined	00	Undefined	00
101	AMB Personality Bytes:Pre-initialization		80		80
102	AMB Personality Bytes:Pre-initialization		20		20
103	AMB Personality Bytes:Pre-initialization	Undefined	00	Undefined	00
104	AMB Personality Bytes:Pre-initialization		44		44
105	AMB Personality Bytes:Pre-initialization		04		04
106	AMB Personality Bytes:Pre-initialization		80		80
107	AMB Personality Bytes:Post-initialization		48		48
108	AMB Personality Bytes:Post-initialization		53		53
109	AMB Personality Bytes:Post-initialization		B3		B3
110	AMB Personality Bytes:Post-initialization		43		43
111	AMB Personality Bytes:Post-initialization		65		65
112	AMB Personality Bytes:Post-initialization		4C		4C
113	AMB Personality Bytes:Post-initialization	Undefined	00	Undefined	00
114	AMB Personality Bytes:Post-initialization		10		10
115	AMB Manufacturer's JEDEC ID Code	Intel	80	Intel	80
116	AMB Manufacturer's JEDEC ID Code		89		89
117	Module ID: Module Manufacturer JEDEC ID Code	Hynix	80	Hynix	80
118	Module ID: Module Manufacturer JEDEC ID Code		AD		AD
119	Module Manufacturing location	Hynix(lchon)	01	Hynix(lchon)	01
120	Module Manufacturing Data (Year)	2006	06	2006	06
121	Module Manufacturing Data (Week)	WW?	Variable	WW?	Variable
122-125	Module Serial Number(Main Lot Number)	Undefined	00	Undefined	00
126	Cyclical Redundancy Code	CRC cover 0~116 byte	E9	CRC cover 0~116 byte	9C
127	Cyclical Redundancy Code	CRC cover 0~116 byte	91	CRC cover 0~116 byte	F7
128	Manufacture part number (Hynix Memory Module)	H	48	H	48
129	Manufacture part number (Hynix Memory Module)	Y	59	Y	59
130	Manufacture part number (Hynix Memory Module)	M	4D	M	4D
131	Component group (DDR2 SDRAM)	P	50	P	50
132	Component group(DDR2 SDRAM)	5	35	5	35
133	Manufacture part number (Module depth)	6	36	6	36
134	Manufacture part number (Module depth)	4	34	4	34
135	Manufacture part number (Module type)	F	46	F	46
136	Manufacture part number (Data width)	7	37	7	37
137	Manufacture part number (Data width)	2	32	2	32
138	Manufacture part number (Die Generation)	C	43	C	43
139	Manufacture part number (Package Materials)	P	50	P	50
140	Manufacture part number (Component configuration)	8	38	8	38
141	Manufacture part number (AMB Manufacturer)	N	4E	N	4E
142	Manufacture part number (AMB Revision)	3	33	3	33
143	Manufacture part number (Hyphen)	-	2D	-	2D
144	Manufacture part number (Minimum cycle time)	C	43	Y	59
145	Manufacture part number (Minimum cycle time)	4	34	5	35
146	Manufacture revision Code (for Component)	Module revision code	00	Module revision code	00
147	Manufacture revision Code (for PCB)	--Module revision code	00	--Module revision code	00
148	DRAM Manufacturer JEDEC ID Code	Hynix	80	Hynix	80
149	Manufacturer JEDEC ID Code		AD		AD
150	Manufacturer specific data (may be used in future)	Intel AMB inform rev0.8	01	Intel AMB inform rev0.8	01
151	Manufacturer specific data (may be used in future)		09		09
152-175	Manufacturer specific data (may be used in future)	Undefined	00	Undefined	00
176-255	Open for customer use	Undefined	00	Undefined	00